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Highly Efficient Transmitter for High Peak to Average Power Ratio (PAPR) Waveforms

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Aethercomm has shown that a high efficiency power amplifier can be developed to enhance efficiency over specific bands over frequencies ranging between 400MHz through 4000MHz with up to 67% efficiencies. These frequencies can be extended down to 30MHz and offer consistent performances by adding additional band functionality allowing support for both HMS, GMR and various commercial applications. The high efficiency power amplifier performance levels shall be maintained with high PAR modulated signals such as multi-carrier, LTE, WiMAX and WCDMA by incorporating Envelope Tracking (ET) functionality in the transmitter. Enhanced signal fidelity can be achieved with the high average output powers by implementing Digital Pre-Distortion (DPD), and Crest Factor Reduction (CFR). With the design implementation proposed, the end product will be a rugged and robust, highly integrated, high efficiency, versatile, state-of-the-art transmitter solution suitable for fixed and mobile military platforms requiring high efficiency RF performance extending between 30MHz through 4000MHz.

15. SUBJECT TERMS

Digital Predistortion (DPD), Crest Factor Reduction (CFR), Envelope Tracking (ET), Class E, Class J, WCDMA, GaN, High Efficiency Power Amplifier

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TABLE OF CONTENTS

Section I:	Overview	1
Section II:	Distortion Mechanisms Overview	6
Section III:	Digital Signal Conditioning	10
Section IV:	Analog Signal Conditioning	14
Section V:	High Efficiency Power Amplifier	20
Section VI:	Linearity Feedback System	32
Section VII:	Power Supply Modulator (Envelope Tracking)	37
Section VIII:	Demonstrated Prototype Results	39
Section IX:	Phase 2 Transition Plan	43
Section X:	Conclusion	45
Section XI:	References	46

SECTION I: Overview

A Wideband High Efficiency Transmitter solution can be achieved with multi-octave RF bandwidths, offering high efficiency and enhanced signal fidelity. The transmitter system will support both simple and complex modulation topologies which can include constant envelope, Global System for Mobile Communications (GSM), Long Term Evolution (LTE) and high peak to average ratios (PAR) modulation topologies like Orthogonal Frequency Division Modulation (OFDM) including Wideband Code Division Multiple Access (WCDMA) and Worldwide Interoperability for Microwave Access (WiMAX) communication standards.

High average output power will be offered in excess of +40.0dBm (10W) while supporting modulation bandwidths up to 20MHz. These features will be offered in the Wideband High Efficiency Transmitter in the form of an integrated transmitter module providing an extremely rugged, robust and versatile communication system platform well suited for harsh military environments. The transmitter core features shall provide the following functionality:

<u>Digital Pre-Distortion (DPD):</u>	Provides Enhanced Signal Fidelity
<u>Crest Factor Reduction (CFR):</u>	Provides Enhanced Efficiency
<u>Envelope Tracking (ET):</u>	Provides Enhanced Efficiency
<u>High Efficiency Power Amplifier:</u>	Provides Enhanced Efficiency over Extended Bandwidths

The system implementation will include state-of-the-art, commercially available components that will interface with a high efficiency power amplifier specifically designed for the transmitter module. The final design shall integrate all components within a single housing enclosure with very small form factors to facilitate use in mobile man-pack applications including Handheld, Manpack & Small Form Fit (HMS) and Ground Mobile Radio (GMR) uses.

With a user specified frequency, the system will automatically select the appropriate frequency sensitive components and tune itself for operation at the desired RF frequency. Utilizing the innovative high efficiency power amplifier design, extended support can be offered many of the Joint Tactical Radio System (JTRS) and commercial broadcast frequencies listed in TABLE 1. The transmitter module shall be responsible for all RF modulation, linearization, amplification and efficiency enhancement responsibilities in an fully integrated solution with an estimated enclosure size of 6.8" x 3.4" x 1.3" as shown in FIGURE 1.

All these features can offer typical spectral enhancement capabilities ranging between 15dBc to 30dBc as illustrated in FIGURE 2 while enhancing efficiencies up to 20% depending on the modulated signal topology.

ACRONYM	DESCRIPTION	FREQUENCY	
		Lower	Upper
		MHz	MHz
ACAS	Avionics Identification, Collision Avoidance and Traffic Alert	1030	1090
DWTS	Digital Wideband Transmission System	1350	1850
EPLRS	Enhanced Position Location Reporting System	420	450
GSM	Global Mobile Communications	380	921
HAVE QUICK	Military Aircraft Radio	225	400
IFF	Avionics Identification, Collision Avoidance and Traffic Alert	1030	1090
LINK	Link -4A, -11B, -16, -22	960	1215
LMR	Land Mobile Radio	25	960
MSS	Mobile Satellite Service	1610	2500
PCS	Personal Communication Service	1850	1990
SATCOM	UHF Satellite Communication	225	400
SATURN	Second Gen. Anti-jam Tactical UHF Radio for NATO	225	400
SINCGARS	Single Channel Ground Air Radio System	30	88
TCAS	Avionics Identification, Collision Avoidance and Traffic Alert	1030	1090
VHF	Air Traffic Control (Civilian)	108	137
Wi-Fi	Wireless Fidelity	2400	2400
WiMAX	Worldwide Interoperability for Microwave Access	2300	3500
WLAN	Soldier Radio and Wireless LAN	1755	2500

TABLE 1: Supported and Expanded Frequency Table



FIGURE 1: Mechanical Form Drawing

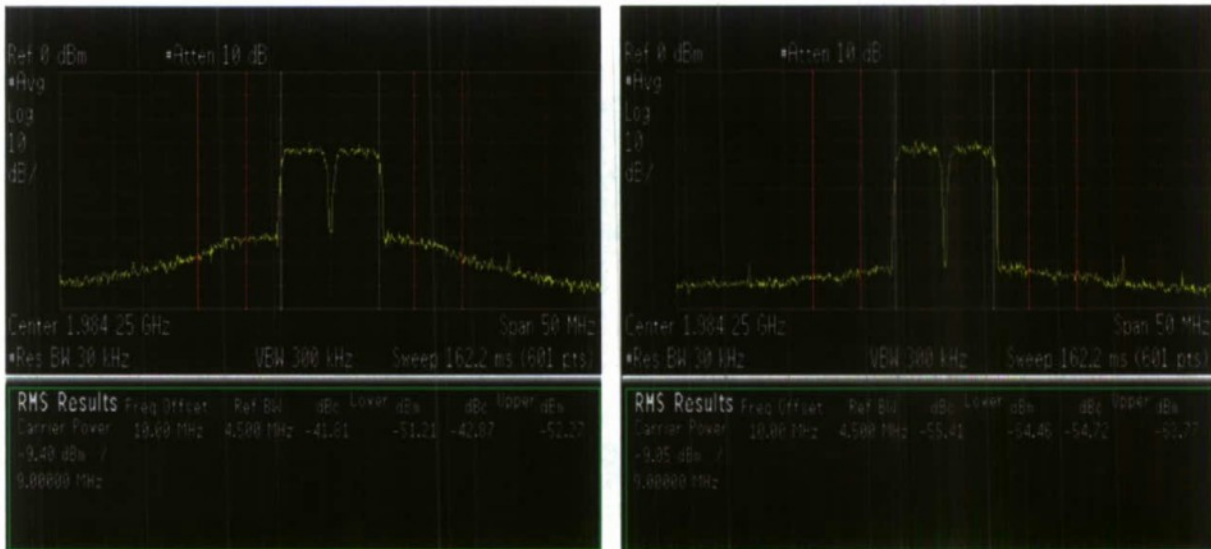


FIGURE 2: Measured Spectral Mask Plots without and with DPD, respectively

The RF modulation, spectral purity and efficiency enhancement capabilities of the transmitter will be offered by integrating five core sub-systems. The sub-systems are digital signal conditioning, analog signal conditioning, high efficiency power amplifier, linearity feedback system and power supply modulator sections. Each of these sections shall be controlled by a microprocessor, enhancing user functionality, versatility and expandability. A detailed block diagram of the complete system implementation is shown in FIGURE 3. The system implementation can be summarized in the following steps with the more detailed implementation discussed in successive sections of this report.

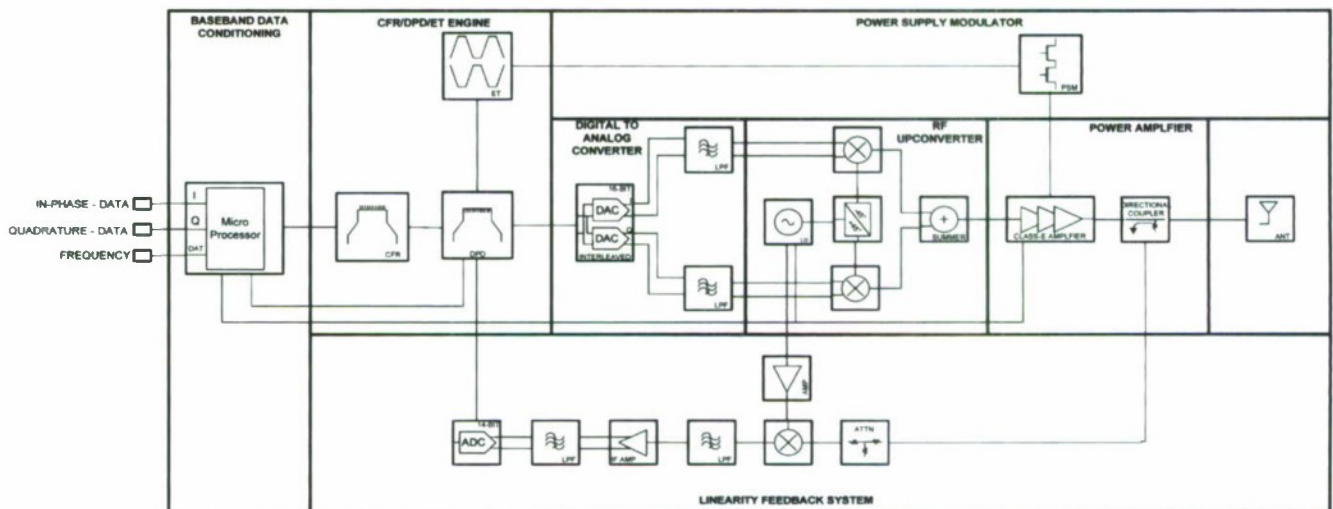


FIGURE 3: Transmitter System Block Diagram

DIGITAL SIGNAL CONDITIONING

1. BASEBAND DATA CONDITIONING: (Microprocessor)
 - a. Accept coded *modulated baseband* in-phase (I) and quadrature (Q) data inputs
 - b. Accept desired transmitter frequency information
 - c. Selects appropriate “frequency selectable” system components
2. CFR/DPD/ET: (Transmit Processor)
 - a. Crest-Factor Reduction (CFR)
 - i. *Modulated baseband* signal characteristics are modified to improve amplifier efficiency and peak power requirements
 - b. Digital Pre-Distortion (DPD)
 - i. *Modulated Baseband* signal is modified to correct the subsequent stages non-linearity contributions
 - ii. Signal correction bandwidth is established and baseband data is offset to an intermediate frequency
 - iii. Post-amplified signal with introduced non-linearity is received and interpreted
 - iv. Correction information sent and received from DSP processor
 - v. Pre-distorted *Modulated Baseband* signal is achieved by applying correction information
 - vi. *Modulated Baseband* signal characteristics are sent to power supply modulator for envelope tracking power amplifier efficiency enhancement

ANALOG SIGNAL CONDITIONING

1. DIGITAL TO ANALOG CONVERTER: (Digital to Analog Domain)
 - a. Pre-distorted *Modulated Baseband* signal is converted to an analog signal
 - b. Sampling rates and signal correction bandwidths are established
 - c. Filtering to remove unwanted signal artifacts
2. RF UP-CONVERTER: (IQ Modulator)
 - a. Desired RF center frequency is received from baseband data conditioner and is synthesized
 - b. *Modulated Baseband* signal is converted to RF frequencies

HIGH EFFICIENCY POWER AMPLIFIER

1. Desired RF center frequency is received from baseband data conditioner and is adjusted as appropriate
2. Accepts modulated RF signal
3. Provides necessary gain to achieve desired output power
4. Enables high efficiency operation
5. Provides rugged and robust solution for military hardware with low heat dissipation

LINEARITY FEEDBACK SYSTEM

1. Amplified signal is sampled to produce feedback reference signal
2. Accepts synthesized RF center frequency for down-conversion process
3. Convert the feedback reference signal down to baseband intermediate frequencies
4. Filter baseband signal to remove feedback path non-linear signal contents and preserve signal integrity
5. Convert reference signal into digital domain using Analog to Digital Converter
6. Sampling rates and signal correction bandwidths are established
7. Provide digital reference signal to digital pre-distortion processor for correction interpretation

POWER SUPPLY MODULATOR (Envelope Tracking)

1. Accepts baseband signal envelope characteristics
2. Adjusts main supply voltage so that it follows the baseband signal envelope characteristics
3. Applies modified supply voltage to the power amplifier

SECTION II: Distortion Mechanisms Overview

The primary mechanisms of non-linearity in a transmitter are gain errors, phase errors and higher order effects including memory effects. These errors are classically defined by amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) distortion which change from instant to instant. FIGURE 4 shows the classical non-linear characteristics of a power amplifier where the gain and phase of the output signal tend not to track linearly with the input signal amplitude and phase characteristics. As a result, the time domain characteristics of the signal do not resemble the intended signal which reduces signal fidelity. These effects can be seen in FIGURE 5 which shows how the effect of AM-AM and AM-PM distortion change the time domain characteristics of a sinusoidal signal.

Since the amplified signal characteristics do not resemble the intended sinusoidal signal, non-linear harmonics are generated by the power amplifier that occurs at multiples of the amplified input frequencies. In single carrier applications, these harmonics can generally be filtered out of the system where the primary effect is a reduction in amplifier efficiency since part power is directed at the unwanted harmonic instead of the desired frequency. However, when amplifying modulated signals, in-band spectral noise is generated along with harmonics that degrade the spectral purity. This in-band noise is classically associated with mixing the main signal with the amplifier harmonics creating “high odd-order” non-linear signals adjacent to the desired signal. Usually, the 3rd order and 5th order non-linearity's tend to dominate in the signal spectrum since their magnitude is the highest. These are the non-linearity's that are targeted for correction by pre-distorters.

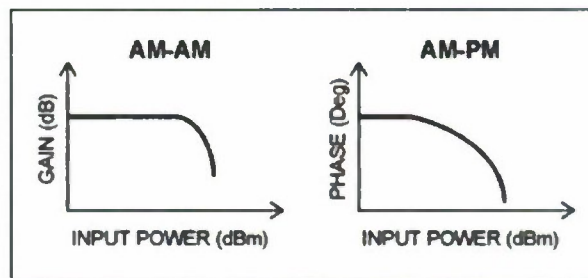


FIGURE 4: Example of AM-AM and AM-PM Distortion Characteristics [1]

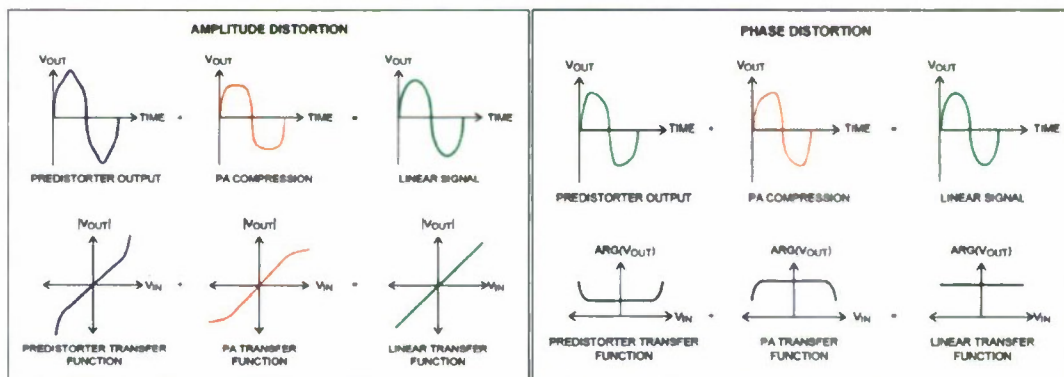


FIGURE 5: Effect of AM-AM and AM-PM Distortion Characteristics [1]

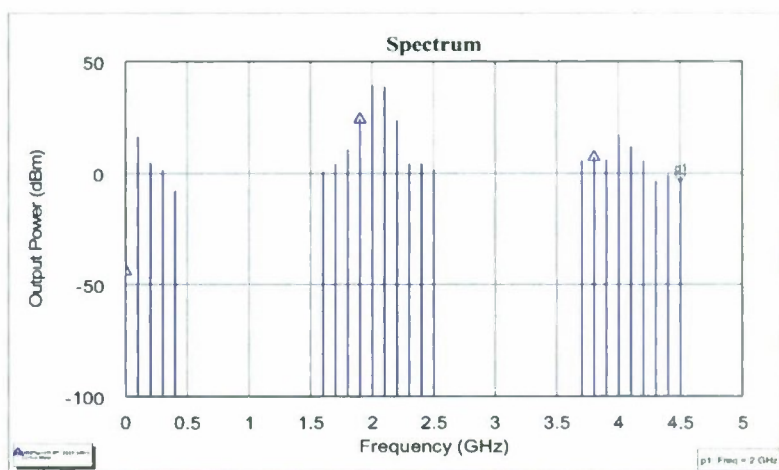


FIGURE 6: WCDMA Spectral Mask for the High Efficiency Power Amplifier

This mixing effect can be demonstrated with a two-tone modulated signal amplified by the high efficiency power amplifier as shown in FIGURE 6 along with up to the 9th order non-linearity's. The desired signals are located at 2.0GHz and 2.1GHz, the 3rd order effects occur at 1.8GHz and 2.2GHz, the 5th order effects occur at 1.7GHz and 2.3GHz and so on. For the multiple-carrier modulated signals shown, these odd-order non-linearity's represent the Inter-Modulation Distortion (IMD) of the amplifier output signal and demonstrate the impact on spectral purity when amplifying modulated signals.

Amplifying complex modulated signal exhibit similar mixing characteristics except the impact is more significant since the in-band noise is spread over a certain modulation bandwidth adjacent to the desired signal bandwidth. This effect can be broken down as shown in FIGURE 7 which shows the spectral components associated with the non-linear mixing products and how it is spread around the desired signal with a 20MHz modulation bandwidth.

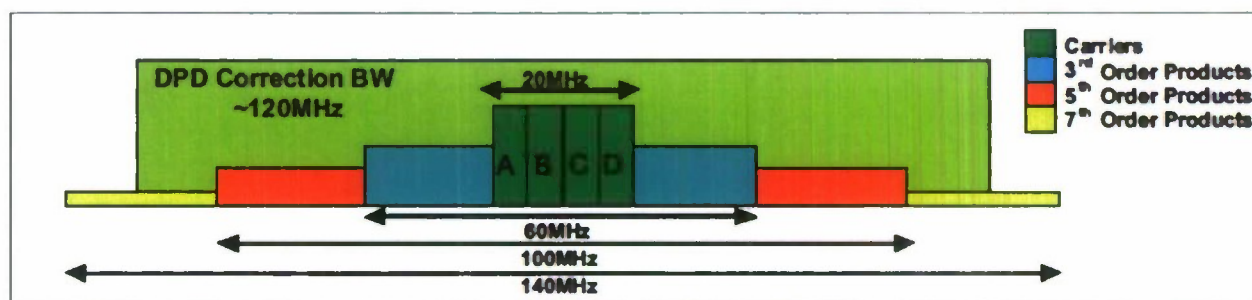


FIGURE 7: Non-Linear Spectral Components [2]

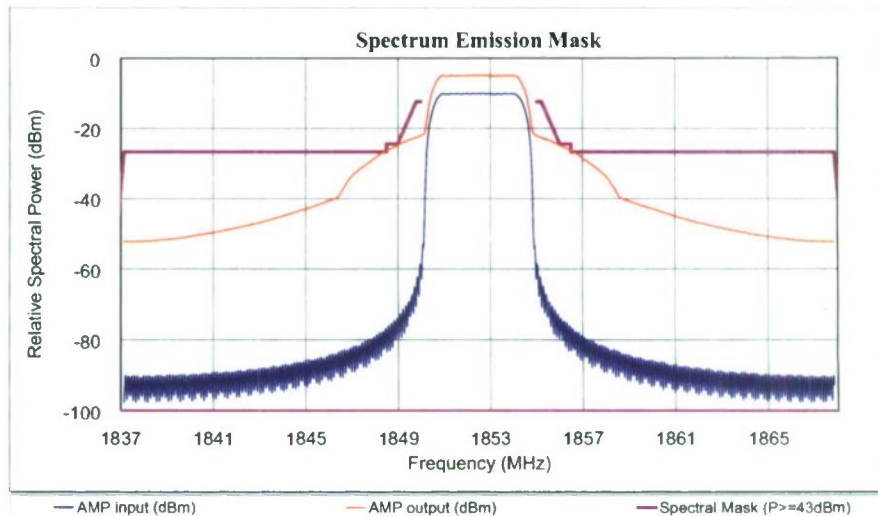


FIGURE 8: WCDMA Spectral Mask for the High Efficiency Power Amplifier

These degradation mechanisms are exhibited by the high efficiency power amplifier when modeled using a WCDMA Test Model 1 signal with 64 DPCH channels operating in the commercial cellular broadcast frequency. The corresponding spectral mask is shown in FIGURE 8 which details the ideal signal characteristics, spectral emissions limits and the amplified signal with its added non-linear noise characteristics. This noise power is characterized by the Adjacent Channel Power Ratio (ACPR) which is the ratio of power in the desired band to the power in the adjacent band.

When using high peak-to-average (PAR) signals, like WCDMA, exhibiting PARs as high as 13dB, thermal and electrical memory mechanisms in transistors further degrade signal fidelity. Thermal memory effects are associated with the instantaneous localized heating in the transistor when amplifying the peak power levels of the modulated signal. This adds additional amplitude and phase perturbations that are not consistent during the next instant the system amplifies the modulated signal at the same amplitude level. Electrical memory mechanisms result from stored charges and non-linear capacitance behavior within the transistor distorting both the amplitude and phase characteristics of the output signal, which again varies from instant-to-instant that the system amplifies the modulated signal at the same amplitude level.

FIGURE 9 details an example of the time-domain characteristics of a WCDMA signal published by Texas Instruments [2] exhibiting memory effects. By correlating the pulses at the 175 and 250 sample interval, which occur at a relatively consistent input amplitude condition, the output signal exhibits larger amplitude and phase deviation (Sample 250) than exhibited in the previous instant the amplitude was at the same level (Sample 175).

To reduce the non-linear contribution by the amplifier and enhance spectral purity, digital pre-distortion (DPD) is added to the modulated signal to anticipate and correct these non-linear effects of the power amplifier. To accommodate the higher order memory effects, this pre-distortion needs to dynamically adapt to the power amplifiers non-linear behavior so that it can be adaptively corrected. This requires a system to feedback the amplified signal, interpret what it should have been and apply the appropriate offsets to the signal to be amplified. These techniques compensate the power amplifiers non-linearity and preserve the original intended signal integrity.

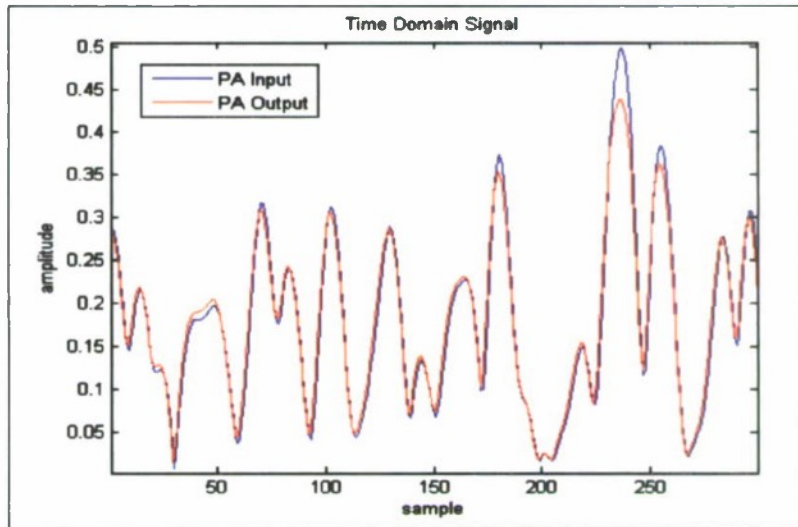


FIGURE 9: Time Domain Characteristics of an Amplified WCDMA Signal [2]

SECTION III: Digital Signal Conditioning

BASEBAND DATA CONDITIONING

The transmitter shall integrate a microprocessor that will accept user defined complex In-phase and Quadrature (I/Q) data encoded for the desired modulation topology intended for transmission. The selected microprocessor is the Actel SmartFusion A2F060M3F1FGG256Y1. The SmartFusion features a microcontroller, a Field Programmable Gate Array (FPGA) and integrated analog functionality. These features provide enhanced versatility and functionality for the Wideband High Efficiency Transmitter by allowing multiple user interface protocols that can be customized based on the necessary platform and application while synonymously controlling the frequency selectable components within the transmitter system.

These functions are offered by the SmartFusion which consists of a 100MHz ARM® Cortex™-M3 processor with an Advanced High-performance Bus (AHB) matrix, system registers, DMA engine, Real-Time Counter (RTC), embedded Nonvolatile Memory (eNVM), embedded SRAM (eSRAM), Fabric Interface Controller (FIC), the Philips Inter-Integrated Circuit (I²C) and 16550 UART (Universal Asynchronous Receiver/Transmitter).

One of the supported communication protocols is a configurable Master or Slave Serial Peripheral Interface (SPI) allowing universal interface methodologies such as Universal Serial Bus (USB). When operating in Master mode, the SPI peripherals generate a serial clock and data to the slave device that needs to be accessed. The SPI peripherals can generate the serial clock from 390 kHz to 50 MHz by dividing the MSS clock, which can be controlled by software. The SPI allows read/write access to all registers that configure external analog to digital converters (ADC) and digital to analog converters (DAC). The microprocessor also allows for I²C that will allow future serial communication protocols with Serial Data Lines (SDA) and Serial Clocks (SCL).

The microprocessor supports a 16550 Universal Asynchronous Received/Transmit (UART) communication protocol. The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM and parallel-to-serial conversion on data characters received from the user. The user can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The microprocessor integrates a large FPGA starting with 1536 tiles of logic on the smallest A2F060 part. The biggest A2F500 device comes with 11,520 tiles. The actual size can be selected based on the intended transmitter application and shows future expandability. Each tile is roughly equivalent to a D-flip-flop or three-input lookup table (LUT). The FPGA sub system can be used for future expansion of the design.

The microprocessor features an integrated 32-bit General Purpose Input/Output (GPIO) interface that will be used to select the frequency selectable components of the transmitter system and accept baseband I/Q signals. GPIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an Input/Output multiplexer (IOMUX).

CREST FACTOR REDUCTION

Crest Factor Reduction (CFR) is a means by which the time domain characteristics of the modulated signal is manipulated in such a way that the PAR is reduced. Implementing CFR improves the efficiency of a transmitter system by allowing the amplifier to operate at higher average power levels without clipping or distorting the modulated signal peaks. Likewise, if a nominal average power level is desired, CFR reduces the overhead needed by the amplifier since the output section does not need to be sufficiently sized to produce the power necessary to amplify the modulated signal peaks. These signal characteristics are shown in FIGURE 10 indicating the signal characteristics for a four-tone modulated signal. Shown are the peak power level, average power level and envelope characteristics of the modulated signal. By applying CFR, effectively the peak power reference line moves closer to the average power reference line reducing peak power overhead requirements.

The Wideband High Efficiency Transmitter shall include CFR functionality by use of the Texas Instruments GC5325 wideband digital pre-distortion transmit processor. The GC5325 includes CFR reduction capability integrated on-chip that is customizable based on the desired PAR reduction. The GC5325 accomplishes CFR by applying a subtracted time domain technique that adds distortion to the signal without altering the signal shape characteristics [2]. This technique has demonstrated CFR reductions on WCDMA signals down to a PAR of 6.5dB. Use of the programmable CFR will require the high efficiency power amplifier to have a peak power capability up to +46.5dBm (45W) to produce an average +40.0dBm (10W) when amplifying a WCDMA signal.

Use of CFR improves system efficiency and reduces power amplifier headroom, but introduces non-linear elements to the intended signal that increases the noise and thus degrading the ACPR. Therefore, the amount of CFR applied to the signal will be software defined based on the peak power capability of the high efficiency power amplifier, the average power requirements and the spectral emission requirements of the transmitted signal.

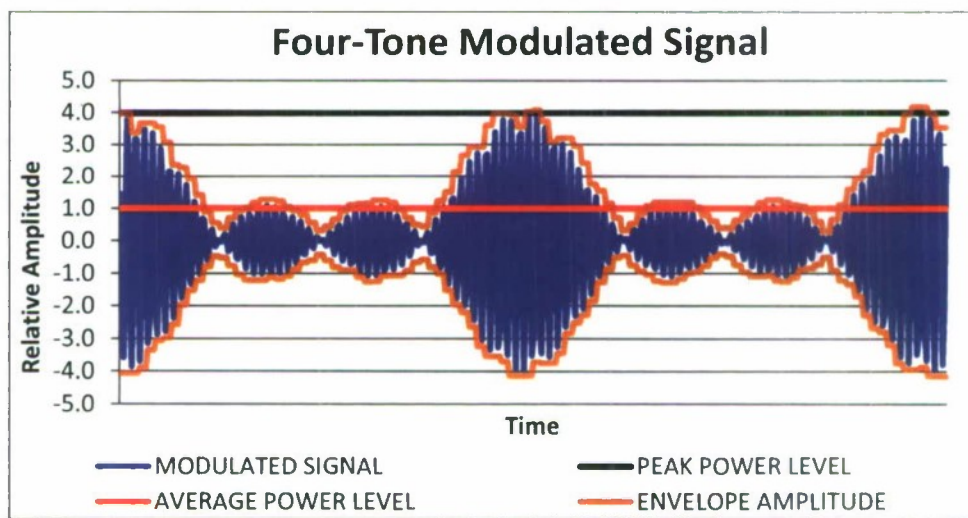


FIGURE 10: Time Domain Characteristics of a 4-Tone Modulated Signal

DIGITAL PREDISTORTION

The Wideband High Efficiency Transmitter shall include adaptive DPD circuitry to maintain the signal fidelity of the amplified signal. This shall be accomplished by the Texas Instruments GC5325 wideband digital pre-distortion transmit processor. This is a high functionality integrated processor that supports typical modulation topologies including all commercial code division multiple access communication standards (WCDMA, TD-SCDMA, CDMA2000), WiMAX, OFDMA and multicarrier signals with up to 20MHz modulation bandwidths and 140MHz “pre-distortion” bandwidths. Pre-distortion is implemented adaptively by evaluating a sampled reference signal from the linearity feedback system which is a signal representative of the amplifier output signal. Appropriate corrections are then applied to the *modulated baseband* signal to correct amplifier-added distortion and enhance signal fidelity.

The GC5325 core implementation is accomplished with the *modulated baseband* input signal, a digital-signal processor (DSP), a digital feedback reference signal representative of the amplifier output signal and a high speed DAC. FIGURE 11 shows a block diagram detailing the implementation approach.

The modulated base-band input signal shall be received from the user by the microprocessor with a modulation bandwidth up to 20MHz. The microprocessor shall pass the data to the GC5325 over an interleaved parallel I/Q data streams and will set the timing interface requirements allowing seamless transition to the transmit processor.

The GC5325 accepts a digital feedback reference signal from an ADC on the linearity feedback system. The ADC interfaces directly with the GC5325 by a parallel digital data-stream. Since the input from the ADC is a real data-stream that does not differentiate the I/Q components, the GC5325 includes a real-to-complex conversion allowing direct signal correlation by an off-chip DSP processor. The reference signal is stored and continuously updated in on-chip data buffers for use with the DSP processor.

Since the feedback reference signal is such an integral part of the DPD functionality, it is important that the reference signal is not further distorted around the feedback path. The GC5325 corrects these non-idealities by including an 8-tap complex equalizer and lookup tables that will ideally account for any additional distortion introduced by the RF-baseband down-conversion process and further enhance correction functionality.

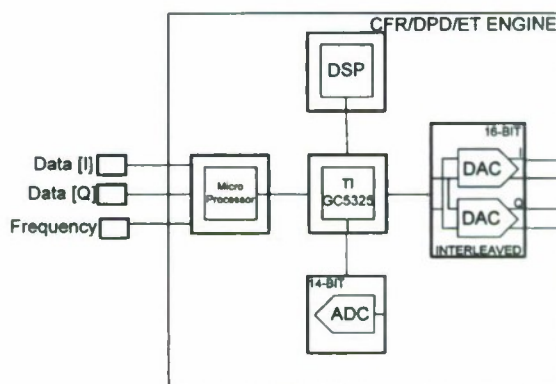


FIGURE 11: Core Implementation Block Diagram for the GC5325

The DSP processor is used to determine the differences between the PA output signal and the intended modulated signal characteristics and apply the appropriate correction terms to it to create a pre-distorted modulated signal. The correction terms are calculated by the DSP circuit and are targeted to improve the AM-AM, AM-PM and memory distortion mechanisms. This method allows correction of several “high order” non-linearity’s depending on the input signal bandwidth, with correction up to 140MHz defining the *pre-distortion bandwidth* of the system as illustrated in FIGURE 7. The DSP circuit operates in asynchronous mode allowing for 16-bit bi-directional data allowing for read and write operations from and too the GC5325 on a continuous basis.

After the 140MHz signal is sufficiently digitally pre-distorted, the signal is presented to an on-chip bulk up-converter where the signal is again up-sampled to expand the signal bandwidth to 210MHz. This functionality enhances DAC filtering and interpolation so that they do not affect the corrected signal.

The GC5325 provides an interleaved serial I/Q data-stream output that represents the pre-distorted modulated signal. This signal interfaces directly to a high speed dual-DAC that converts the modulated signal from the digital domain to the analog domain. The DAC functionality provides an individual analog data-stream representing the in-phase and quadrature signal characteristics to an I/Q modulator that up-converts the signal to the user specified RF frequency.

With the implementation discussed, the transmitter will be capable of accepting user defined baseband signals with 20MHz modulation bandwidths and applying DPD correction to it. The DPD correction will reduce amplifier-added distortion up to 140MHz total bandwidth. Texas Instruments has demonstrated this functionality on their GC5325 System Evaluation Kit, the GC5325SEK. Published improvements on their system platform have shown an ACPR improvement of -30dB when using a WCDMA TM1-64DPCH signal with 3.84MHz modulation bandwidth [2]. The system evaluation kit has also demonstrated ACPR improvements of -16dB when using two WiMAX signals with a total of 20MHz modulation bandwidth and is shown in FIGURE 12 [3].

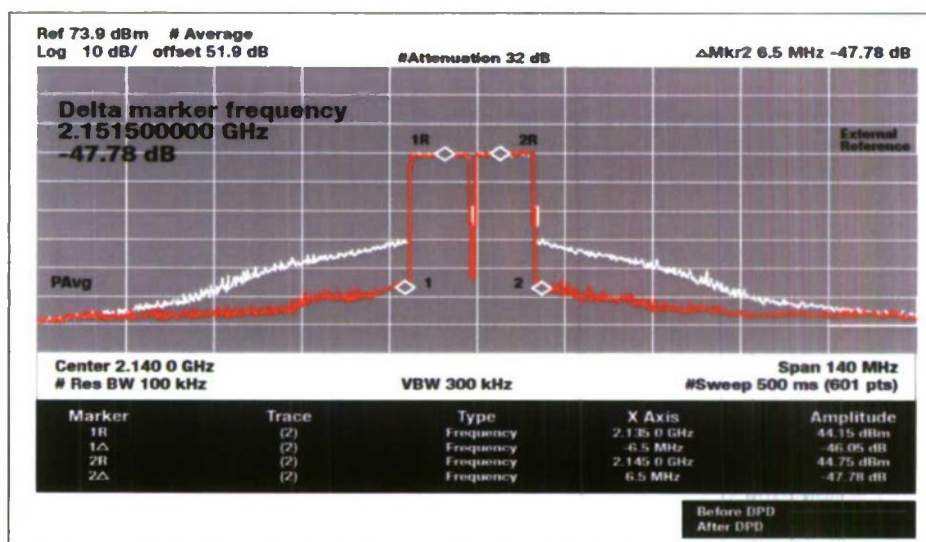


FIGURE 12: Linearity Improvements by use of the GC5325 System Evaluation Kit [3]

SECTION IV: Analog Signal Conditioning

DIGITAL TO ANALOG CONVERTER

Once the base-band data is properly conditioned using the digital CFR and DPD techniques discussed, it is necessary to convert the signals to the analog domain. It is in the analog domain that the information is converted to RF frequencies and then transmitted. The Wideband High Efficiency Transmitter shall accomplish this by integrating a high speed digital-to-analog (DAC) converter.

Since the DAC effectively produces an analog representation of the modulated signal, its performance characteristics must be scrutinized in order to ensure production of a high fidelity signal. Careful selection of the DAC with very low noise, high linearity and high speed characteristics is critical since it sets the dynamic range of the transmitter. The chosen DAC for the Wideband High Efficiency Transmitter is the Analog Devices AD9122.

The AD9122 is a 16-bit dual-DAC solution that interfaces directly with the GC5325 and provides up to 16-bit resolution. The DAC accepts an interleaved I/Q data-stream representing the digital pre-distorted modulated signal. It automatically separates and converts the signal into individual I and Q channels for use by subsequent stages. It includes a novel integrated x2/x4/x8 interpolator which allows for multi-carrier synthesis allowing transmission of multiple modulated channels and reduced filtering requirements.

The DAC shall be configured to interpolate each channel by “x4” which effectively up-samples the 210MHz signal by a multiple of 4 allowing the DAC to operate at a sample rate of 840MSPS on each channel. Having high sample rates are necessary to ensure aliasing does not occur upon analog signal reproduction which is ultimately governed by the Nyquist criteria. As such, the Nyquist criterion is used to set the baseline DAC sampling rate that requires the sampling frequency of the DAC to be at-least twice that of the modulated signal bandwidth.

As a consequence of signal sampling, images of the signal are created above and below the sampling frequency and its harmonics as is illustrated in FIGURE 13. When used with the AD9122 set at x4 interpolation, the 210MHz signal has an image above and below 840MHz. Having the sample frequency 4 times higher than the intended signal, the unwanted images will not overlap and can be sufficiently attenuated using analog filters after the DAC.

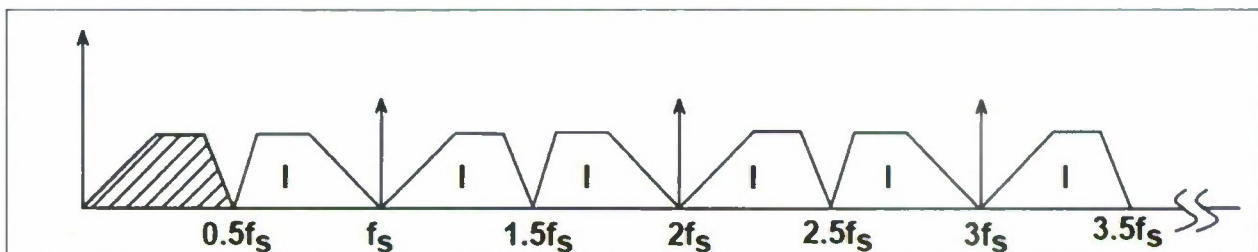


FIGURE 13: Illustration of Sample Frequency (f_s), Image Frequencies and Nyquist Zones [4]

The DAC effectively produces a quantized analog signal defined by the input I and Q data. In the case of the AD9122, a 16-bit word is used to define the amplitude of the analog signal with a resolution up to 27uV defined by 65,536 states. This is the capability of a 16-bit DAC ranging over an output voltage of 1.8V which is represented by 2^{16} possible states.

With such a fine resolution, it is important to ensure the distortion characteristics of the DAC are as low as possible. Integral non-linearity (INL) and differential non-linearity (DNL) are used to identify quantization errors associated with the output signal amplitude. The AD9122 presents an INL of +/-3.7 bits and DNL of +/- 2.1 bits which defines the output amplitude error of up to +/- 108uV and state change errors of 54uV respectively.

Selection of a high fidelity, low noise DAC is important to ensure that the output noise spectrum of the analog signal is low. The AD9122 was designed specifically for wireless infrastructure applications using WCDMA, WiMAX, LTE signals. Spurious Free Dynamic Range (SFDR), Noise Spectral Density (NSD), IMD's and ACPR are used to identify the fidelity of the analog signal. With signal bandwidths up to 210MHz, the AD9122 is advertised [5] with a SFDR of -72dBc, harmonic distortion less than -60dBc, worst case NSD less than -157dBm/Hz and IMD's less than -70dBc. This describes the single and multi-carrier dynamic range of -70dBc by use of this DAC.

Since an objective is to transmit complex modulation architectures, a low output noise spectrum should be considered for modulated signals. The AD9122 is advertised [5] with producing an ACPR of -66dBc while generating a multi-carrier, 4-tone WCDMA with composite bandwidth of 16MHz. Likewise, the AD9122 is advertised [5] with producing an ACPR of -76dBc while generating a single-carrier, 1-tone WCDMA signal with a composite bandwidth of 3.84MHz. The spectrums are shown in FIGURE 14 for each test signal cases respectively.

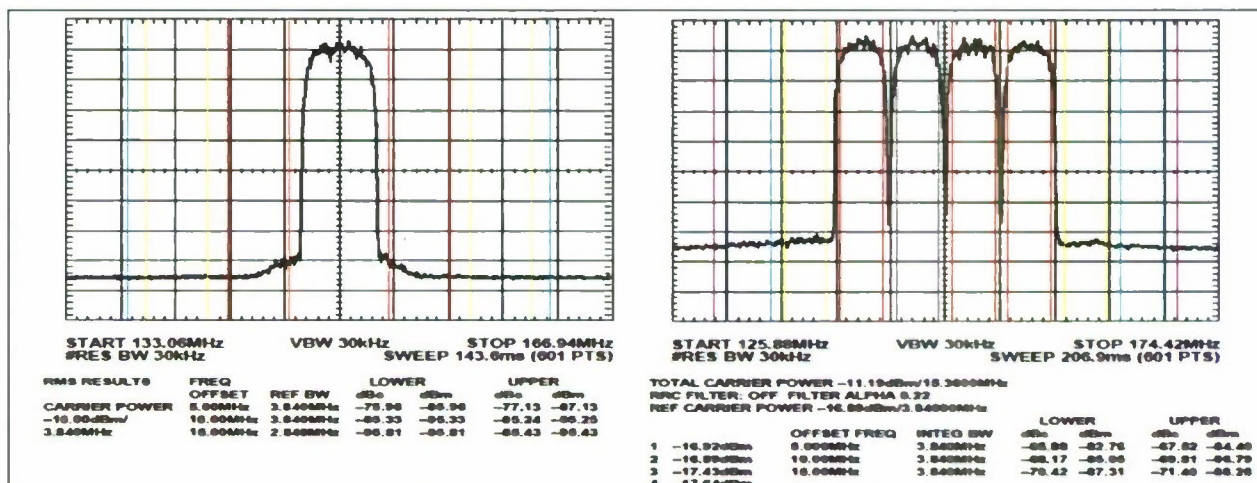


FIGURE 14: Spectral Plot for Single and Multi-Carrier WCDMA Signals Produced from the ADI AD9122 [5]

BASEBAND ANTI-ALIASING FILTERS

After the baseband signal is converted in the analog domain by the DAC, the images need to be appropriately attenuated before the signal can be up-converted to RF frequencies. Image rejection is accomplished using a low-pass filters (LPF) with appropriate stop-band attenuation.

The stop-band attenuation is determined based on the worst case dynamic range of the DAC and was advertised to be -66dBc for a 4-tone WCDMA signal. The frequency at which the stop-band attenuation is achieved, is selected based on the cross-over points between the LPF and its image. This is illustrated in FIGURE 15. With the DAC operating at a sample frequency of 840MSPS and an input signal bandwidth of 210MHz, the LPF must begin attenuation at 210MHz and achieve -66dB of rejection at 420MHz.

The chosen filter topology is a minimum inductor elliptical LPF since it exhibits very low pass-band group delay and very high stop-band rejection characteristics. To satisfy the filter requirements, a 7th order Elliptic LPF was designed and is subsequently shown in FIGURE 16. The filter was realized using discrete lumped elements by arranging two filter structures in parallel to accommodate the DAC's differential output. The filter reduces components by achieving symmetry with respect to the center capacitors by presenting a common electrical reference. Using commercially available inductors and capacitors from Coilcraft and American Technical Ceramics (ATC), the filter rejection requirements were achieved by presenting a corner pass-band frequency up to 210MHz and a -75dB rejection at the image at 420MHz. The pass-band response is shown in FIGURE 17.

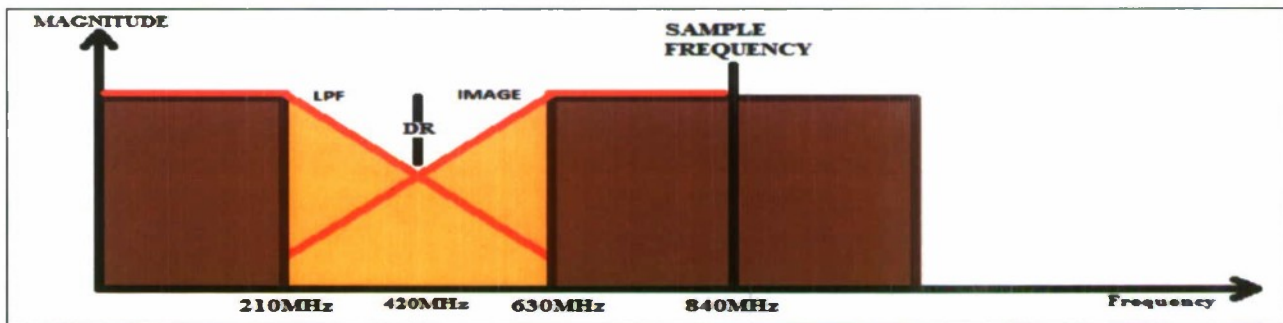


FIGURE 15: Filter Rejection Requirements

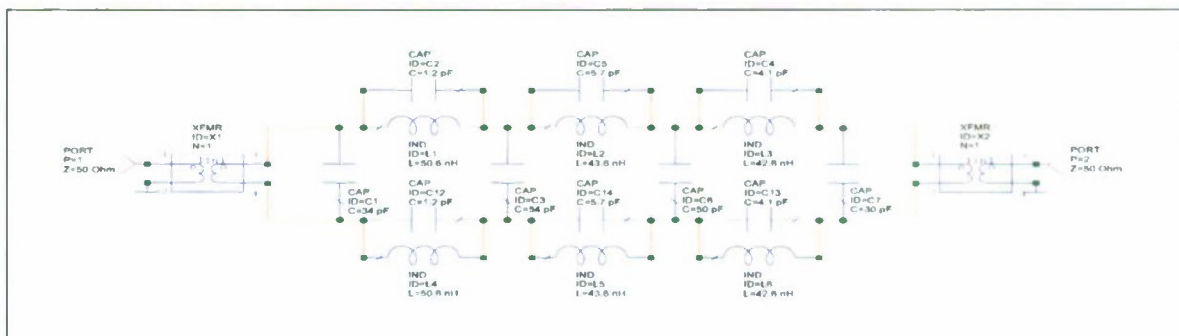


FIGURE 16: DAC Low-Pass Filter Design

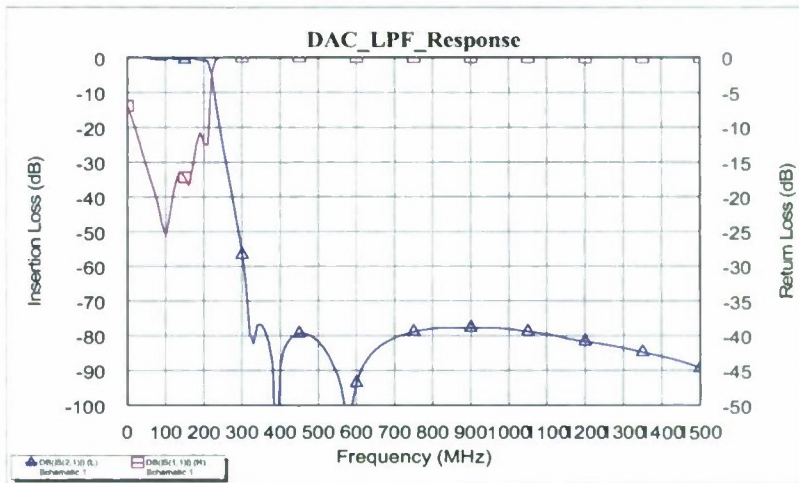


FIGURE 17: DAC Low-Pass Filter Response Characteristics

RF UP-CONVERSION

The next step is to convert the filtered modulated base-band analog signal up to RF frequencies where it can be amplified by the high efficiency power amplifier and transmitted. This is accomplished through an IQ modulator, where each in-phase and quadrature analog signals are mixed with an RF reference frequency and summed together. FIGURE 18 shows the basic block blocks involved in the up-conversion process.

The Texas Instruments TRF372017 shall be used as the broadband IQ modulator. This is a highly integrated device that incorporates a built in fractional frequency synthesizer, buffer amplifiers, polyphase filter and mixers. The device allows direct RF modulation with the base-band signal with RF frequency selectivity in 1Hz increments ranging between 300MHz through 4800MHz with the on-chip frequency synthesizers. The TRF372017 features a high output power capability ideal for driving the input of the high efficiency power amplifier. Additional features include side-band suppression, carrier feed through suppression, digital DC offset control for enhanced carrier feed-through rejection, high linearity and low harmonic distortion.

The on-chip frequency synthesizers, work by synthesizing the desired RF transmit frequency using the on-chip phase-lock-loop (PLL) and voltage-controlled-oscillator (VCO). Based on the frequency specified by the user, the PLL is set for the appropriate RF frequency and locks the VCO to it defining the local oscillator (LO) frequency. The LO interface is passed through a polyphase filter which splits the local oscillator into two signals with a 90 degree phase variation between them. The polyphase filter facilitates the in-phase and quadrature RF frequencies necessary to compliment the I/Q base-band signal. The base-band and LO signals are then combined in the mixer which presents an in-phase and quadrature modulated RF frequency at the intended transmit frequency. These two signals are then passed to an on-chip RF summer which presents a single ended output for amplification by the high efficiency power amplifier. The IQ modulator also provides a buffered LO output frequency to be used by the Linearity Feedback System.

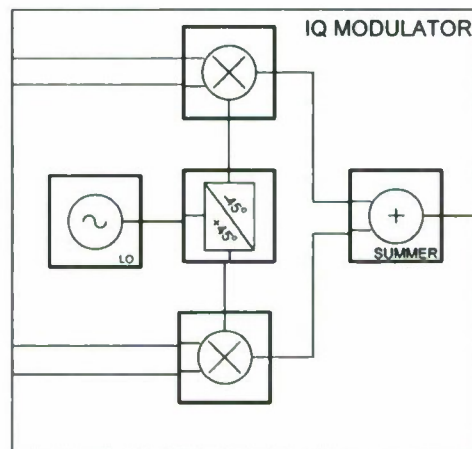


FIGURE 18: Block Diagram of the IQ Modulator

The TRF372017 has the capability of bypassing the internal frequency synthesizers and utilizing an external frequency synthesizer for extended bandwidth capability. By use of this feature, the transmitter can be expanded to support frequencies ranging between 30MHz through 4800MHz. To extend the frequency range below 300MHz down to 30MHz, external frequency synthesizers from Synergy Microwave will be used utilizing the LFSW2476-10 and FSW1857-100 parts. These synthesizers have a frequency response of 240MHz to 760MHz and 180MHz to 570MHz respectively. The LFSW2476-10 will drive a divide-by-8 prescaler from Hittite Microwave corporation utilizing the HMC363S8G yielding a synthesized LO frequency ranging between 30MHz through 95MHz. Likewise, the FSW1857-100 will drive a divide-by-2 prescaler from Hittite utilizing the HMC361S8G yielding a synthesized LO frequency ranging between 90MHz to 285MHz. The appropriate synthesizer will be selected using the Hittite HMC197A RF switch commanded by the microprocessor depending on the desired frequency of operation. The output will be presented to the TRF372017 external frequency input for up-conversion purposes thus fully supporting transmission down to 30MHz.

Signal integrity is maintained by the high linearity properties of the TRF372017. The device is advertised [6] with an ACPR of -75dBc while producing a single-carrier, 1-tone WCDMA signal. This matches the dynamic range of the AD9122 output with only 1dB signal degradation. Furthermore, noise contribution by the IQ modulator is low, which exhibits a noise floor better than -153dBm/Hz and a worst case closed loop phase noise of -90dBc/Hz when measured 1kHz from the carrier. These built in features maintain the signal fidelity prior to amplification and minimize mixer induced distortion mechanisms.

SECTION V: High Efficiency Power Amplifier

To achieve the high efficiency power amplifier, the design shall facilitate Class-E operation which is a switch mode power amplifier topology that is theoretically able to achieve 100% efficiency using ideal devices and operating under ideal conditions. Class-E operation achieves these theoretical efficiencies by facilitating the transistor device as a switch while manipulating the current and voltage waveforms at the transistor drain. The objective is to offset the phase of the voltage and current waveforms so that when there is a voltage present on the transistor drain, the transistor is switched off and thus does not conduct current. Since power is the product of voltage and current, no power is dissipated in the transistor which allows all the supply power to be utilized at the output antenna.

The output matching network achieves the necessary voltage and current phase offsets by presenting specifically tuned output circuits. These circuits present the transistor drain an inductive output impedance and an appropriate shunt capacitor while applying a series resonant circuit in-line with the transistor output as discussed by Cripps [9]. The inductive output impedance offsets the voltage and current phase so that they do not overlap while the shunt capacitor maintains RF currents through the series resonant circuit during the period that the transistor is switched off, allowing power at the desired RF frequency to be realized at the power amplifier output.

The disadvantage of Class-E operation is that typical RF bandwidths are less than 40%. To achieve enhanced bandwidth operation, different tuned circuits specifically optimized for the intended band of operation shall be switched into the Class-E amplifiers output network. This was chosen in comparison to switching in multiple Class-E amplifier's that were individually tuned to specific frequency segments, because output switching losses can exceed 1dB and thus reduce efficiency as much as 16%.

To facilitate switched tuning networks, parallel tuning elements are desired due to the high power handling requirements of the high efficiency power amplifier. This helps incorporate electronic switches since they present low parasitic properties that can be more easily absorbed in the tuning networks themselves when used in parallel configurations. The best suited Class-E amplifier design topology for the high efficiency power amplifier design is detailed in [10] with the intended approach illustrated in FIGURE 19. The main objective of the parallel resonant tuning elements is to present an inductive load to the transistor with constant phase delay across frequency. The challenge shall be to satisfy this objective over the intended RF bandwidth utilizing commercially available components.

In an effort to determine the appropriate RF transistor to be operated in a Class-E mode, it is necessary to find a device that can withstand voltages in excess of three times the supply voltage. Due to these high voltages, devices with very high breakdown voltages are needed. Furthermore, to extend the upper operating frequency limit, the transistor must be selected as to minimize its intrinsic parasitic properties. Since the desired shunt output capacitor needed to achieve Class-E operation decreases with higher frequencies, minimizing the drain capacitance is of particular importance.

The best suited technology is Gallium Nitride (GaN) since its wide band-gap properties offer breakdown voltages greater than 100V while operated at a nominal 28V supply. GaN transistors exhibit relatively low on-state resistance which enhances efficiency operation since the device can continue to conduct current at low drain voltages. Additionally, GaN transistors also exhibit low drain capacitance maximizing its frequency potential.

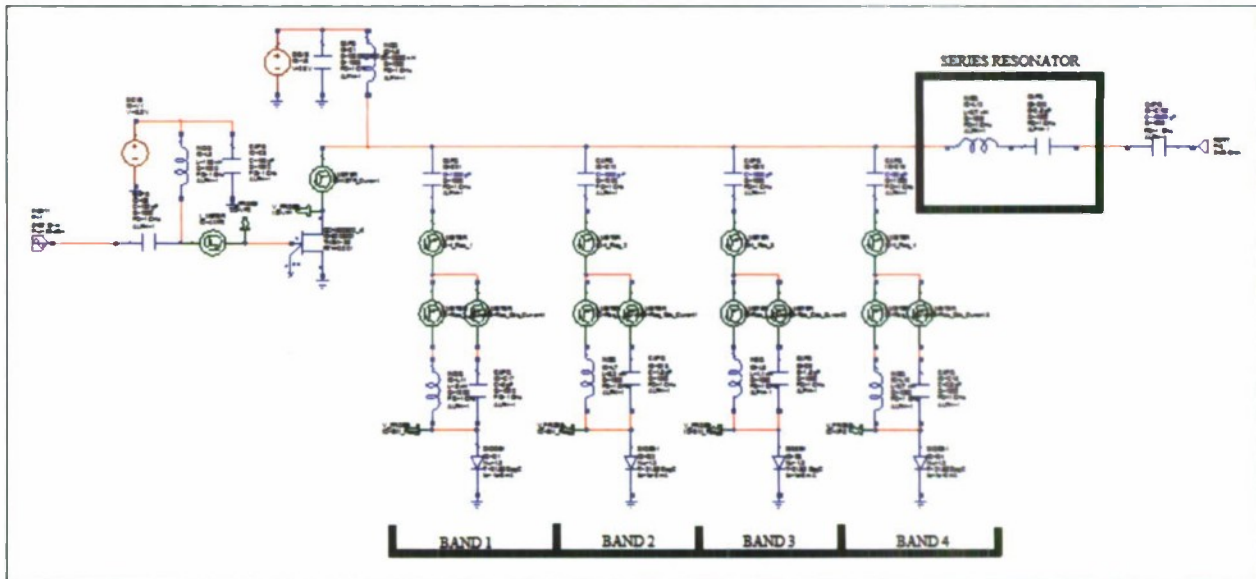


FIGURE 19: Wideband Class-E Amplifier Topology

After scrutinizing the device properties of the leading GaN manufactures, the Cree CGH60030D device proved to be the best choice due to its high breakdown voltage of 100V, low on-state resistance of 1.3-ohms, low drain capacitance of 1.3pF and Cree's refined manufacturing process extending from September 2007 for this device alone.

The CGH60030D is a 30W transistor device and shall serve as a building block where more devices can be combined to increase the power capability of the overall power amplifier. This device size served as the best candidate for high frequency operation since Class-E operation is sensitive to transistor output capacitance. To maintain Class-E operation up to 6000MHz, ideally drain capacitances should be limited below 1.0pF. Thus, use of larger devices will result in significantly higher drain capacitances which will restrict Class-E operation to below 4000MHz while use of smaller devices would incur more combining losses and thus decrease system efficiency.

In order to establish baseline performance using physically realizable transistors and ideal circuit parameters, the Cree CGH60030D transistor was modeled with various tuned Class-E output circuits. The goal was to establish the maximum achievable performance so that all subsequent work can address any deviation from this baseline. By using the physical model of the transistor, the device non-idealities are automatically considered. Baseline performance results were modeled under ideal switching considerations, where each appropriate band resonator was switched into the circuit and all others disabled from the model. The series resonator was re-tuned for the center frequency of each band during the corresponding analysis. Baseline results for efficiency and output power were determined and are summarized in FIGURE 20. The results are evaluated for a single frequency carrier with amplifier operation at saturated output power. This serves as the upper limit boundary detailing the peak power and efficiency capabilities from the device.

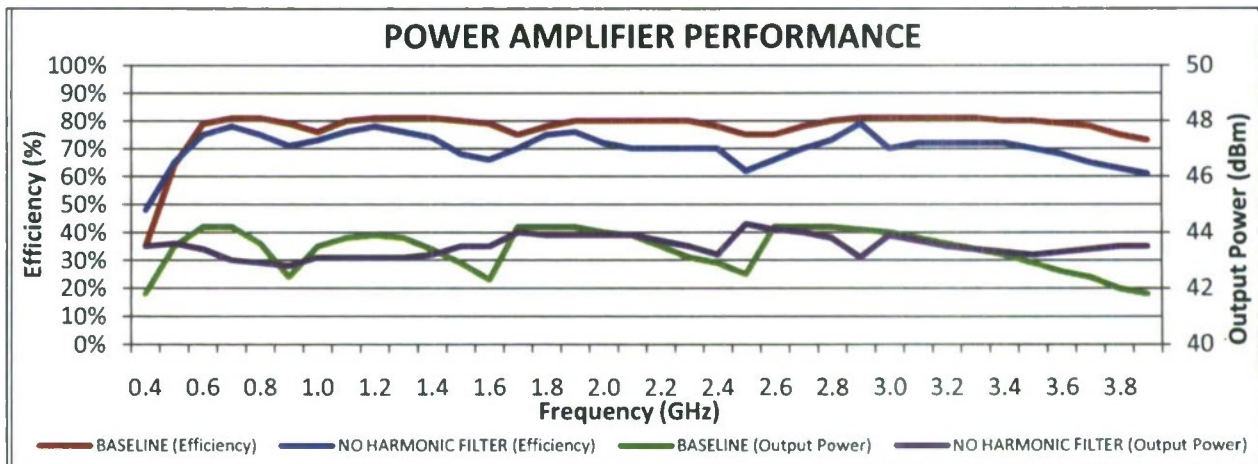


FIGURE 20: Baseline Performance Results of the Switched Class-E Amplifier

It was found that each resonant tuning structure provided up to 50% bandwidth while maintaining high efficiency operation. Therefore, to extend the target bandwidth of 400MHz through 4000MHz, a minimum of four resonant structures were necessary. The corresponding bands were delineated as follows:

- Band 1: [0.4 to 0.9] GHz
- Band 2: [1.0 to 1.4] GHz
- Band 3: [1.5 to 2.2] GHz
- Band 4: [2.3 to 3.9] GHz

As can be seen from the results summarized in FIGURE 20, typical drain efficiencies of 80% can be achieved over all bands with output powers ranging between +42.5 to +44.5dBm. These results show that under ideal conditions, excellent bandwidth potential is possible from this implementation of the Class-E power amplifier while concurrently achieving very high efficiencies.

To validate that the design implementation is controlling the drain voltage and current waveforms properly, the time domain characteristics were evaluated and are shown in FIGURE 21 for Band 2 and Band 3 at 1200MHz and 2000MHz respectively. From the curves, desired Class-E operation is achieved since overlap between the drain voltage (Black Trace) and the drain current (Blue Trace) is minimized while the shunt capacitor currents (Brown Trace) sustains the desired sinusoidal currents after the transistor drain current discontinues to conduct and drops to zero. Consistent waveforms were observed for Band 1 and Bands 4 and are therefore not shown.

Since the Wideband High Efficiency Transmitter design objectives require the power amplifier to support high output power levels necessary to sustain the peak power requirements of the modulated signal, a major challenge was encountered in accommodating a tunable series resonant circuit over the entire frequency range. As a result, a modified analysis was conducted without the series resonant circuit to determine the efficiency impact without the resonator. The power amplifier performance is shown in FIGURE 20 yielding a typical drain efficiency of 70% showing a reduction of 10% across the entire evaluated frequency range. One solution to address this is to electronically switch in different series resonant circuits, however series switching losses can be as high as 1dB, resulting in a 16% efficiency reduction from the power amplifier. Therefore, since no practical solution can be included in the design, subsequent work shall utilize the results obtained without the series resonant circuit as the baseline.

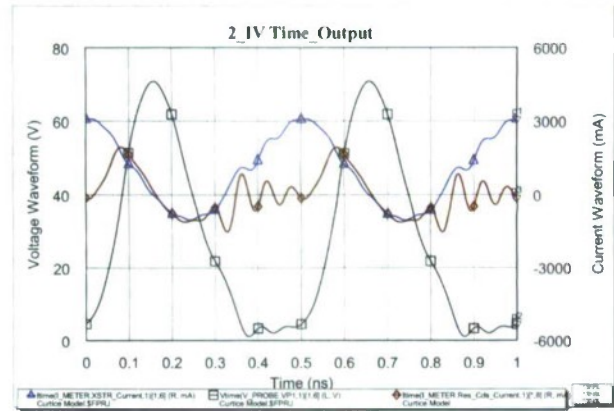
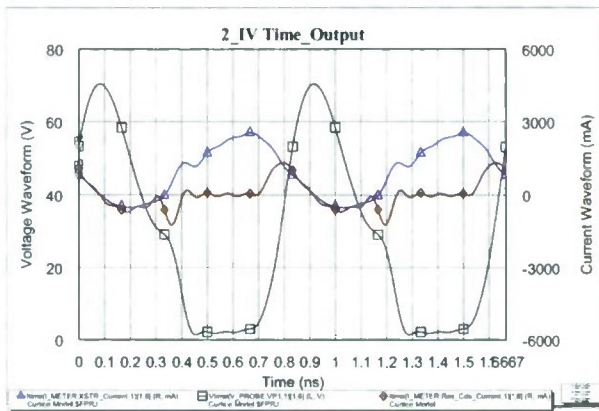


FIGURE 21: Transistor Drain Voltage and Current Waveforms for Band 2 and Band 3

To determine the cause of the efficiency reduction, the drain voltage and current waveforms were re-evaluated without the series resonant circuit and are shown in FIGURE 22. From the curves, increased distortion is present on the drain voltage and current waveforms which result in an increased overlap of the drain voltage and currents and more power directed to the non-linear components resulting in the decreased efficiency.

These distortion mechanisms are more easily identified by evaluating the harmonic components of the waveforms as illustrated in FIGURE 23 for Band 2 and FIGURE 24 for Band 3. The corresponding results show an increased second harmonic voltage of 5dB resulting in more harmonic distortion as seen by the transistor drain without the use of the series resonator in the output network.

The next step in the design was to determine how each bands tuning network could be switched into the circuit. Two options were considered, where one option was to use RF transistors and the second option was to use high frequency diodes.

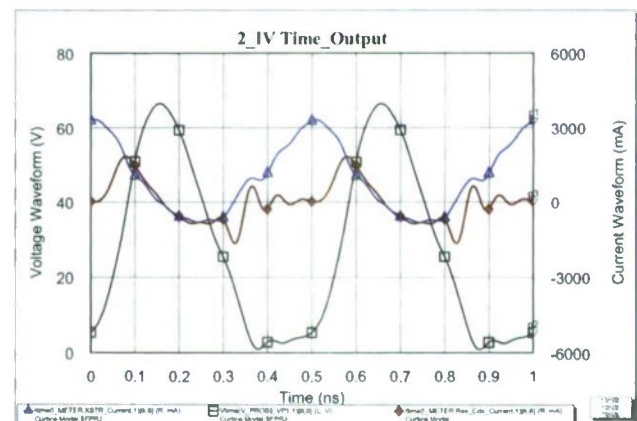
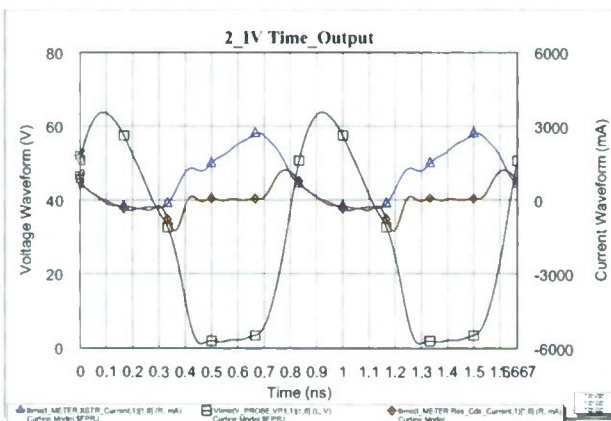


FIGURE 22: Transistor Drain Voltage and Current Waveforms for Band 2 and Band 3

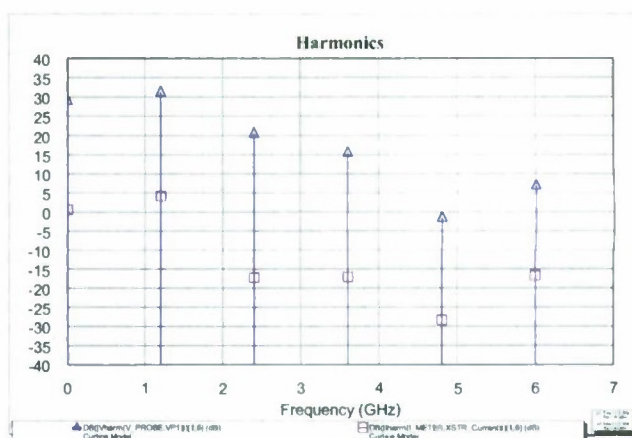
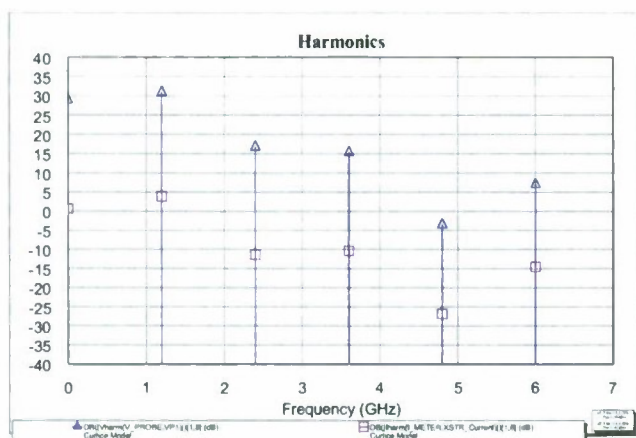


FIGURE 23: Transistor Drain Harmonics for Band 2 without and with Series Resonator, respectively

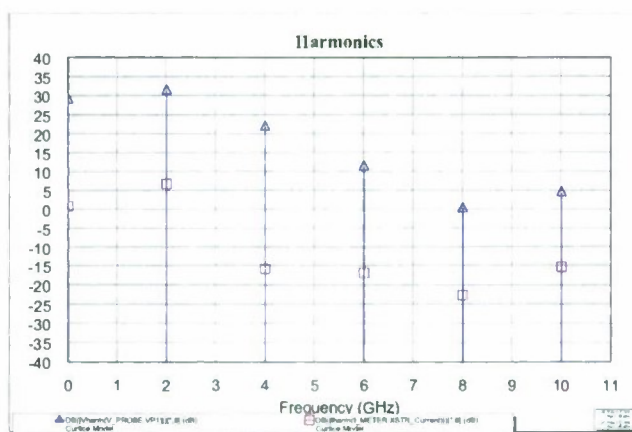
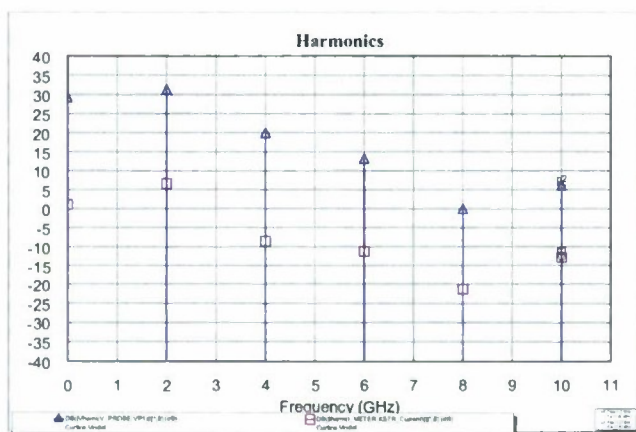


FIGURE 24: Transistor Drain Harmonics for Band 3 without and with Series Resonator, respectively

To determine the best technology choice to facilitate shunt switching for the corresponding parallel tuning networks, it is necessary to minimize off-state series capacitance and on-state resistance from the switching element itself. The switching elements on-state resistance causes power to be dissipated in the active bands tuned circuit and thus decreased efficiency as a result of a lower quality factor parallel resonant circuit. Likewise, the switching elements off-state capacitance causes unwanted currents to be conducted through the disabled bands parallel tuning circuits which decrease efficiency of the active band.

Diode switching will lend itself to highest amplifier efficiency over using transistors as switching elements. This is a direct result of the diodes lower off-state capacitance and lower on-state resistance, where both parasitic parameters are at-least 66% lower.

With the diode switch technology implementation, the power amplifier efficiency and output power was evaluated using a detailed physical model. The model includes all transmission lines necessary to physically incorporate each bands parallel tuning circuits into the network and allow the transistor to deliver power into a 50-ohm output termination. The transmission lines are realized using Alumina Oxide substrates with gold as the conductor. The diodes are included in the model utilizing S-parameters for a representative diode.

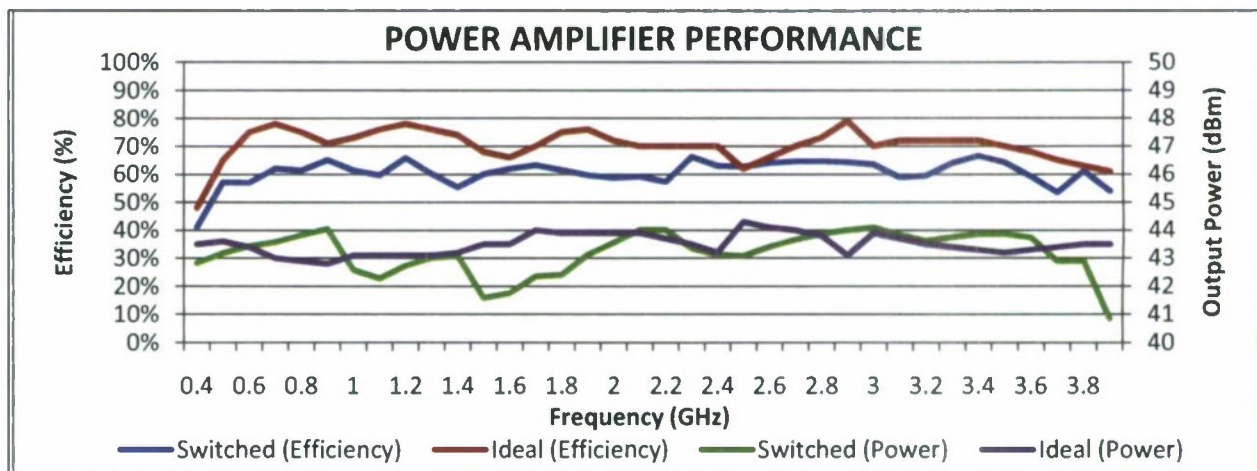


FIGURE 25: Baseline Performance Contrasted with Diode Switches

Using diode switch elements result in a typical efficiency of 60% showing a reduction of 10% across the entire evaluated frequency range as shown in FIGURE 25. To determine the cause of the efficiency reduction, the drain voltage and current waveforms were re-evaluated and are shown in FIGURE 26 for comparison to the desired waveforms shown in FIGURE 22. From the curves, increased distortion is present on the drain voltage and current waveforms which result in an increased overlap of the drain voltage and currents resulting in the decreased efficiency.

These distortion mechanisms are more easily identified by evaluating the harmonic components of the waveforms as illustrated in FIGURE 27 for Band 2 and Band 3. When compared with the harmonics shown in FIGURE 23 and FIGURE 24, implementing diode switches change the harmonic behavior significantly. The most impacted is the second harmonic showing a reduction in voltage and current of 15dB. By examining the curves, it is evident that physical implementation utilizing diode switch elements do not sustain Class-E operation. Instead, a harmonic environment is provided to the transistor drain that more closely facilitates a Class-J high efficiency operating mode as detailed in [9].

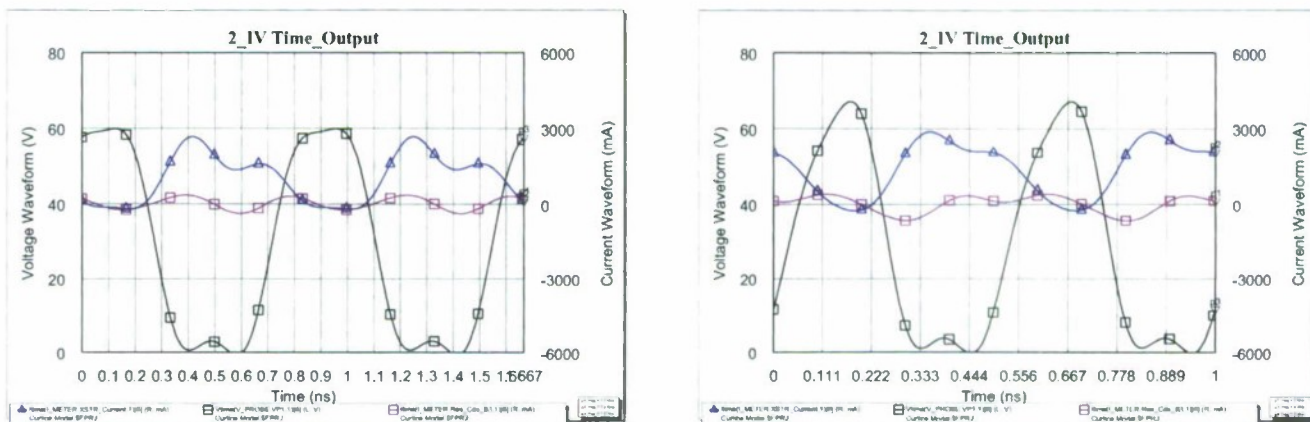


FIGURE 26: Transistor Drain Voltage and Current Waveforms for Band 2 and Band 3

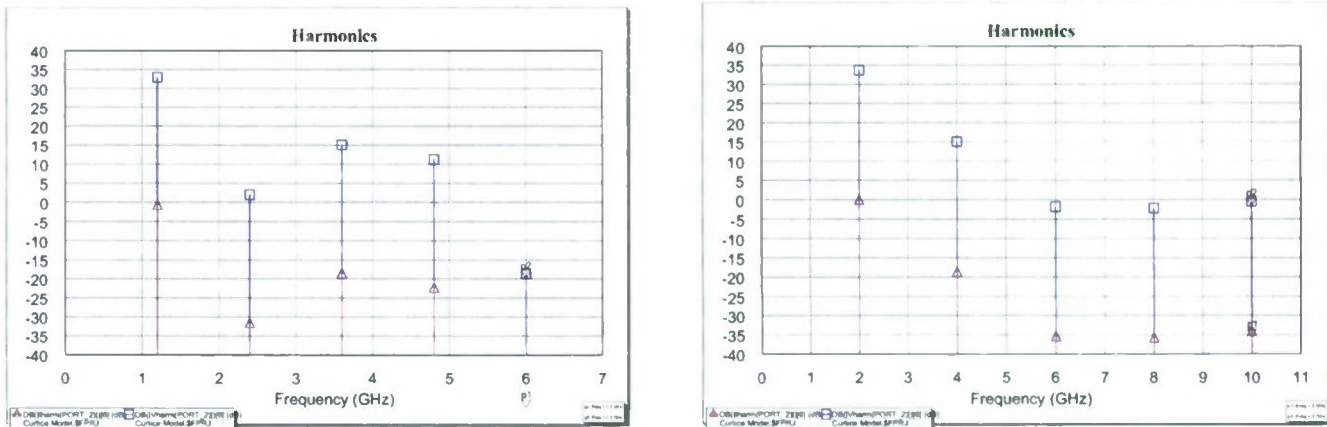


FIGURE 27: Transistor Drain Harmonics for Band 2 and Band 3 while Enabled

It is worth noting that even though the efficiency of the high efficiency power amplifier ranges between 41% and 67%, these results yield performances that are still considerably higher than commercially available MMIC devices. As a baseline comparison, the Cree CMPA0060025F is a broadband MMIC device capable of producing 25W between 20MHz to 6000MHz. This device yields efficiencies that range between 31% and 55% over the same evaluated frequency range.

To evaluate the expected performance of the high efficiency power amplifier with modulated signals, the amplifier was modeled with a two-tone signal (PAR: 3dB). The corresponding results for both efficiency and power are shown in FIGURE 28. This test signal can be used to represent GSM modulation architectures which all consist of similar PARs.

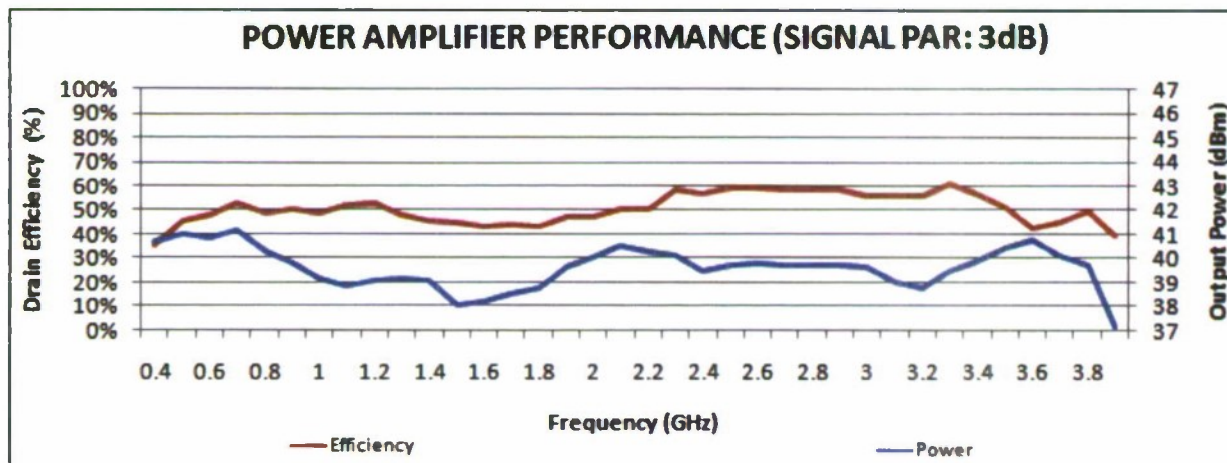


FIGURE 28: Performance Evaluated with a Two-Tone Modulated Signal (PAR: 3dB)

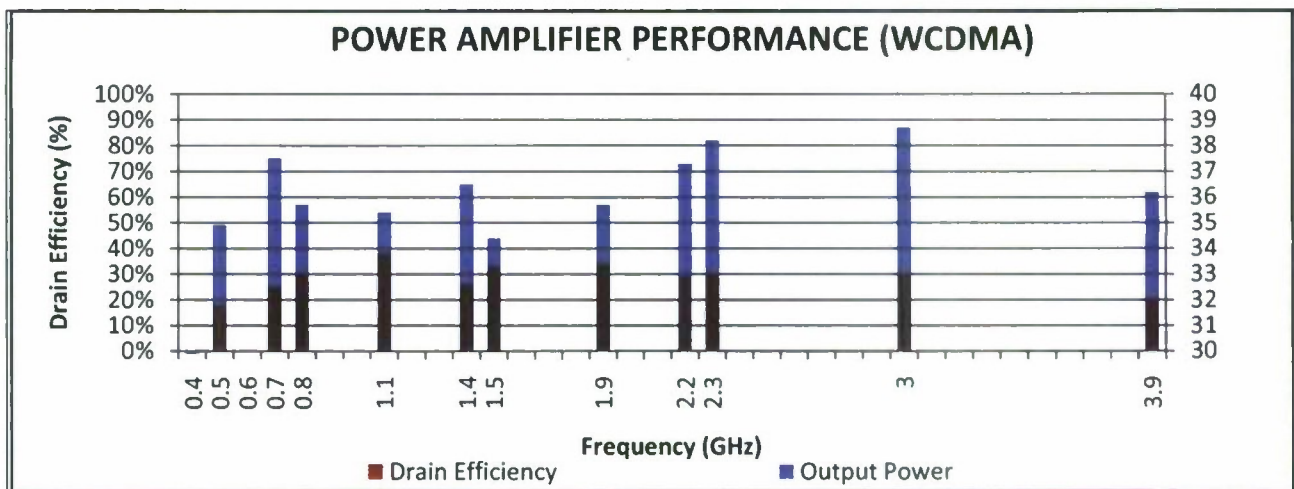


FIGURE 29: Performance Evaluated with a WCDMA Modulated Signal (PAR: 13dB)

The performance of the high efficiency power amplifier was modeled with complex modulated signals such as a WCDMA TM1 (64-DHCP) signal with a 3.84MHz modulation bandwidth (PAR: 13dB) with up to 6dB CFR. The corresponding results for both efficiency and power were evaluated at discrete frequencies within each band are shown in FIGURE 29. This test signal can be used to represent performance with various high PAR complex modulation architectures including WiMAX. From the results, expected efficiencies are 30%.

To achieve the modeled performance results, the high efficiency power amplifier needs at-least 4W of RF drive out to 4000MHz. At lower frequencies, less power is required due to the high gain characteristics associated with GaN transistors. This drive requirement shall be satisfied by using two CGH60008D transistors which is effectively a scaled version of the CGH60030D. Each CGH60008D will drive a pair of CGH60030D devices. This driver shall be tuned and biased for Class AB operation to provide multi-octave bandwidths while simultaneously maintaining higher linearity and good efficiency. Two low power GaAs pre-driver devices from Hittite Microwave Corporation, the HMC634LC4, shall be used to amplify the 1mW signal from the RF up-converter and drive the CGH60008D. A simplified block diagram of the total high efficiency amplifier system is shown in FIGURE 30.

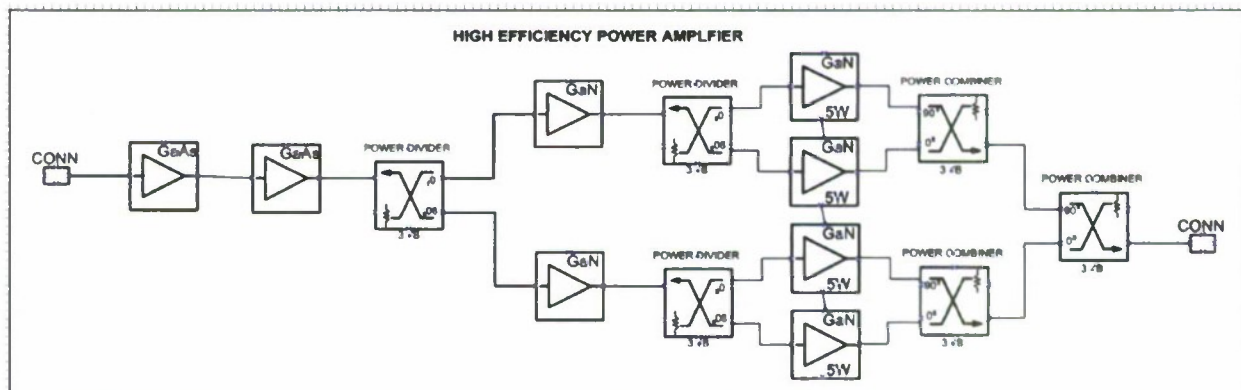


FIGURE 30: Simplified Block Diagram of the High Efficiency Power Amplifier

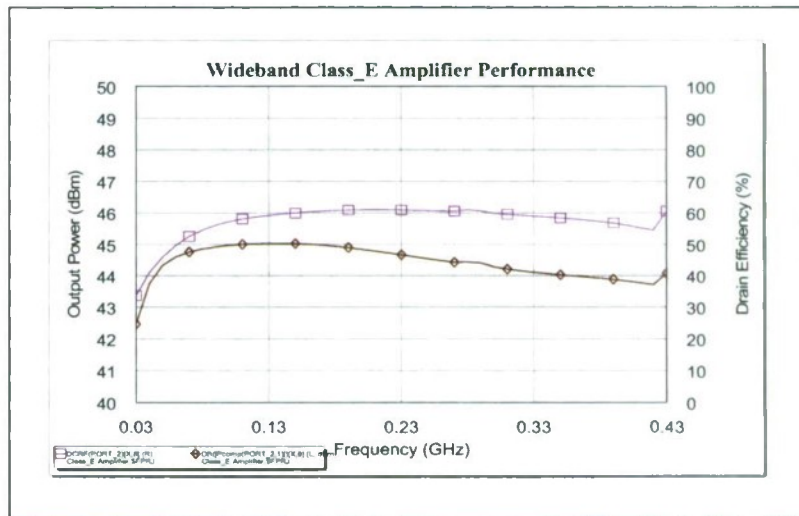


FIGURE 31: Enhanced Frequency Range Performance Results

To demonstrate the capability of the high efficiency power amplifier to support enhanced frequency range down to 30MHz, the design was modeled by turning off each frequency band tuning structure. Modeled performance revealed that the amplifier can provide typical efficiencies greater than 50% at output power levels of +44dBm (25W) provided that the DC decoupling capacitors are increased to a minimum of 300pF and the output transformer bandwidth is extended. The corresponding extended frequency performance results are shown in FIGURE 31 showing that the frequencies listed in TABLE 1 could be supported with some design modifications.

MECHANICAL CONSIDERATIONS

Since the intended application of the Wideband High Efficiency Transmitter is to support commercial and military applications including JTRS HMS and GMR mobile man-pack systems, a thermal management and space study analysis was considered to determine the packaging requirements and thermal considerations for the high efficiency power amplifier sub-system. In this study, only the power amplifier was evaluated since this is the part of the system that dissipates the most power and is most significantly affected by thermal management.

The most stringent operating condition will support modulation topologies with up to 13dB PAR imposing a 6dB CFR requiring four combined high efficiency power amplifiers to achieve the target output power. This configuration will require the most housing space. To include all digital and analog circuitry in an integrated housing module, the components shall be configured into two separate levels where the upper level shall enclose all digital circuitry, power supply modulator and the RF up-conversion and down-conversion components. The lower level shall enclose the entire high efficiency power amplifier including driver and filtering circuitry. The exploded view of this configuration is shown in FIGURE 32. The corresponding housing requirements can occupy an estimated space of 6.8" x 3.4" x 1.3" corresponding to the outline drawing shown in FIGURE 33.

Based on the housing requirements, a thermal study was completed to determine the reliability of the transistors and diodes. Characteristic of most military hardware, the base-plate temperature was evaluated at +85C using an infinite heat capacity surface. The corresponding thermal rise through the components was evaluated based on the dissipated power through the device and its thermal resistance. With the amplifier lineup discussed in the preceding section for a single high efficiency power amplifier output stage, a thermal model was constructed with the initial conditions shown in TABLE 2. The corresponding thermal profile is shown in FIGURE 34 and summarized in TABLE 2.

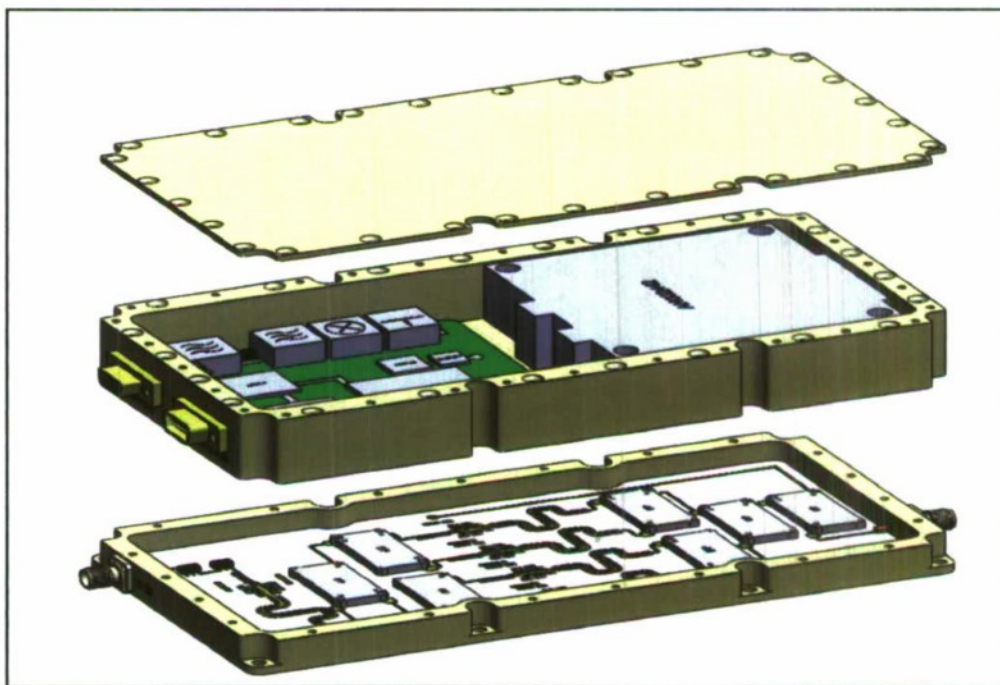


FIGURE 32: Mechanical Space Study

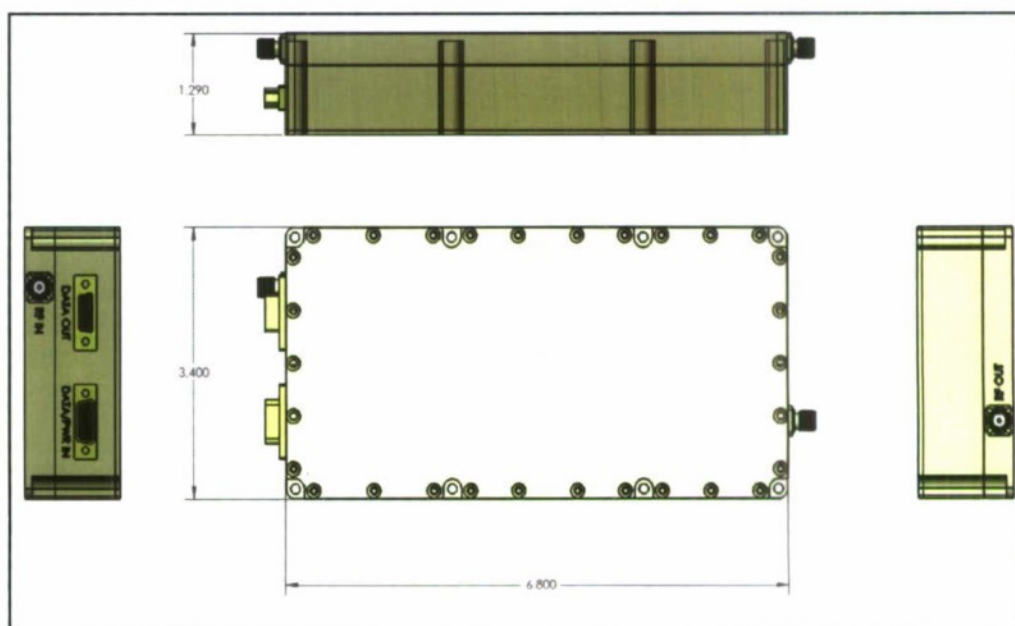


FIGURE 33: Mechanical Outline Drawing

Based on the corresponding analysis, the CGH60030D shows a transistor junction temperature less than 180 °C. Cree devices offer reliabilities greater than 1 million hours at junction temperatures of 225°C and below providing a very rugged amplifier for the Wideband High Efficiency Transmitter. When operated at this temperature, the device will yield an estimated reliability greater than 1 million hours. Consequently, the diode shows a junction temperature in excess of 127 °C and will yield an estimated reliability greater than 1 million hours as well. With these results, the high efficiency power amplifier will provide a rugged and robust part of the transmitter demonstrating it is well suited for mobile man-pack applications because of its very small mechanical outline and very high reliability even at base-plate temperatures in excess of +85°C.

Device	Power Dissipated	Thermal Conductivity	Base-Plate	Housing Temperature	Device Temperature	Estimated Reliability
<i>Units</i>	<i>W</i>	<i>°C/W</i>	<i>°C</i>	<i>°C</i>	<i>°C</i>	<i>Hours</i>
Power Amplifier (CGH60030D)	24	2.2	85	127	180	>1 million
Driver Amplifier (CGH60008D)	8	8.8	85	103	173	>1 million
Diode	2	10.0	85	107	127	>1 million

TABLE 2: Thermal analysis properties

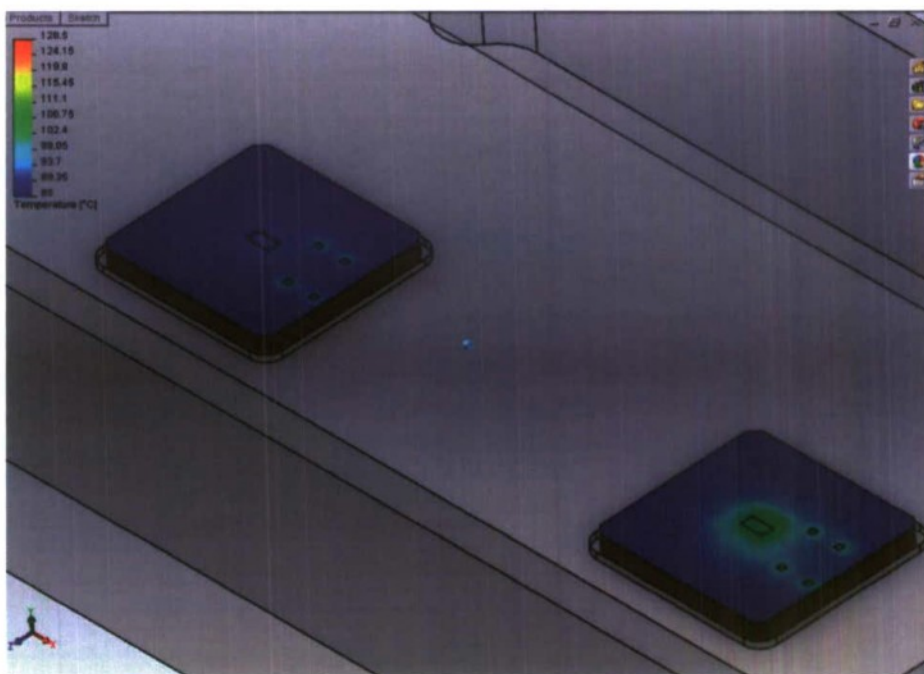


FIGURE 34: Transistor Thermal Analysis Study

SECTION VI: Linearity Feedback System

In order to adaptively pre-distort the amplified signal, the Texas Instruments GC5325 needs to sample and interpret the RF signal produced after amplification by the high efficiency power amplifier. Since the amplified signal is at RF frequencies, it needs to be sampled, down-converted back to baseband and quantized in the digital domain. Shown in FIGURE 35 is the block diagram detailing the stages involved in feeding back the amplified signal to the GC5325.

The first step in signal conversion is to sample the RF amplified signal after amplification by the high efficiency power amplifier. This shall be accomplished by the use of a wideband directional coupler that will extend over RF frequencies ranging between 400MHz through 4000MHz. The directional coupler shall be the Innovative Power Products IPP-8043. This is a custom product made specifically for the Wideband High Efficiency Transmitter and is capable of sustaining peak power levels of 100W. The directional coupler is a surface mount structure that will be placed in-line with the high efficiency power amplifier combiner assembly and the antenna as shown in FIGURE 3. The coupler shall introduce no more than 0.25dB insertion loss on the main path ensuring that transmitter efficiency reduction is no more than 4%. The coupler shall produce a sampled RF signal that is 45dB below the main signal level with a flatness of ± 0.75 dB across the desired frequency range minimizing amplitude errors across frequency. Directivity shall be greater than 20dB ensuring that output impedance reflections do not significantly distort the sampled signal. The IPP-8043 directional coupler performance characteristics are shown in FIGURE 36.

The coupled signal shall then be passed to a digital attenuator that will be uniquely selected to ensure that the peak power level of the sampled signal is sufficiently backed off from the next stage to prevent distortion. The Hittite HMC792LP4E is a digitally controlled, 6-bit attenuator providing a 0.25dB step size across frequencies ranging between 30MHz through 6000MHz. The microprocessor will automatically control the attenuation needed for optimum DPD correction.

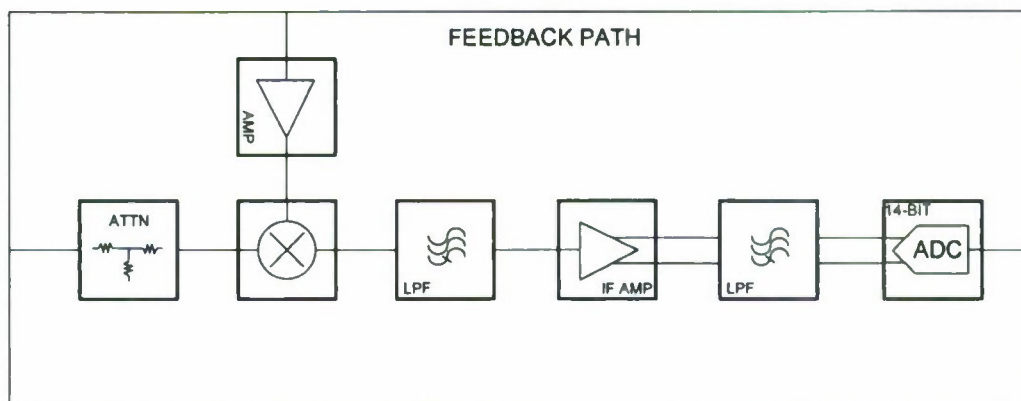


FIGURE 35: Feedback Path Block Diagram

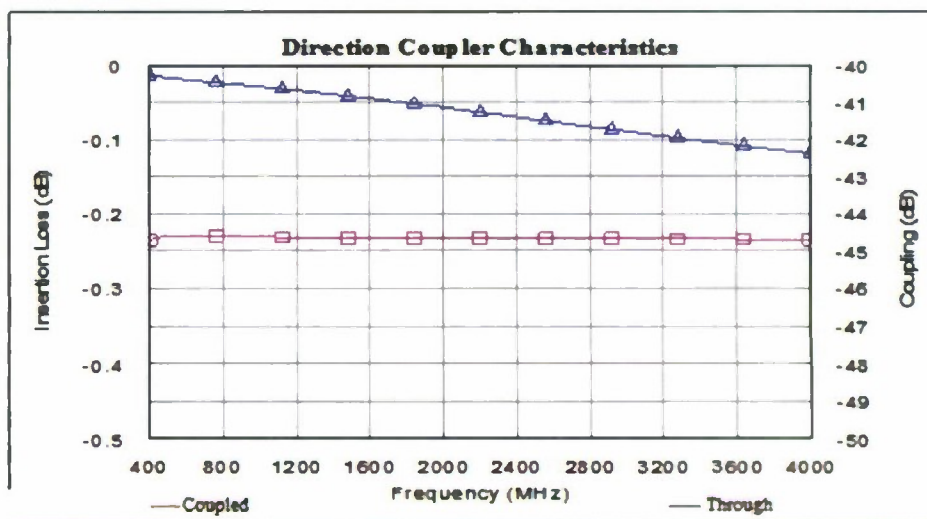


FIGURE 36: The IPP-8043 Directional Coupler Performance Characteristics

The attenuated coupled signal shall then be passed to a wideband double balanced mixer for signal down-conversion back to base-band. The Pulsar Microwave XL-11-A will be used for this process since it is a single ended device that offers a frequency response extending between 1MHz through 6000MHz.

To convert the signal back to the original base-band frequency, the XL-11-A will be driven by the same LO frequency used by the TRF372017 IQ modulator as it mixes the sampled RF signal back down to base-band. The IQ modulator supports this requirement by providing a buffered output reference frequency from the internal PLL/VCO frequency synthesizer which is used in the on-chip mixers. For applications between 30MHz through 300MHz, the external frequency synthesizers shall be passed to a broadband resistive T power divider network. One branch will provide the LO signal for the IQ modulator and the other shall provide the LO signal for the XL-11-A.

Use of a double balanced mixer sustains feedback signal linearity because this mixer topology inherently provides very low spurious products during signal conversion. In order to achieve these low products, high LO drive levels need to be applied to the mixer LO input. The Hittite HMC460LC5 shall be used to sufficiently amplify the LO signal prior to the XL-11A LO input since it offers an extremely flat gain response between 30MHz through 6000MHz while providing up to +18dBm saturated output power levels.

To enhance feedback signal fidelity; spurious products, harmonics, images RF leakage and LO leakage must all be sufficiently attenuated before the signal is converted into the digital domain by the analog to digital converter (ADC). A LPF used after the mixer shall be used to attenuate these out-of-band spurious products, harmonics and leakage signals. The filter shall be designed using a 7th order elliptical filter with a corner frequency up to 210MHz to ensure very high stop-band rejection. The filter implementation and pass-band characteristics are shown in FIGURE 37.

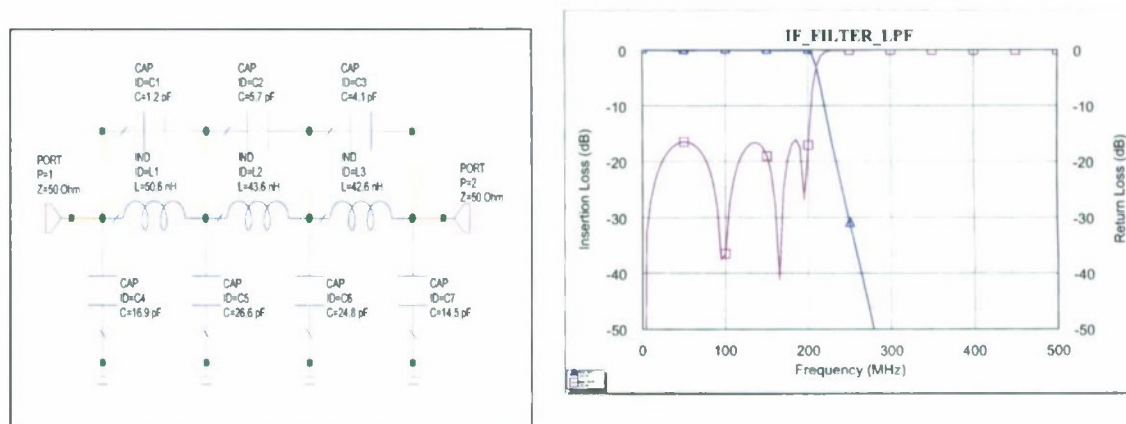


FIGURE 37: Base-Band Low-Pass Filter

The filtered down-converted signal shall then be passed to an IF amplifier that will buffer the impedance interaction between the next stage and the mixer. The Analog Devices ADL5561 shall be used for this process since it offers flat gain and power characteristics through 210MHz. The device provides a single ended to differential signal conversion allowing it to seamlessly interface the mixer with the ADC. It has an integrated digital attenuator to be used for further amplitude control. This maintains appropriate dynamic range of the ADC while ensuring that added distortion isn't introduced due to signal overdrive. The IF amplifier maintains signal integrity by offering very linear properties exhibiting high OIP3 of +40dBm and low harmonic distortion below -60dBc. Lastly, to further attenuate out-of-band spurious products and reject any additional non-linear elements, the same LPF filter shown in FIGURE 16 shall be used after the IF amplifier prior to the ADC.

Using this analog feedback path, the spectral content was modeled to show the signal level and distortion that will be presented to the ADC. The LO frequency was set as 105MHz below the RF frequency yielding an IF frequency of 105MHz. Shown in FIGURE 38 is the out-of-band spurious emissions of the mixer and shows that the output signal content sufficiently attenuates all products down to -156dBc ensuring negligible distortion on the intended signal. Shown in FIGURE 39 are the in-band spurious emissions of the mixer and shows that the worst case spur is as much as -60dBc located at 210MHz. Having this much dynamic range between the desired signal center frequency at 105MHz and the unwanted noise at 210MHz ensures that the GC5325 has a high fidelity reference signal to which DPD correction can be accurately interpreted and applied with a noise power density reduction limit of -60dB.

Since accurate DPD correction functionality is predicated on the integrity of the feedback signal characterized in the digital domain, the reference signal must be digitally quantized with high precision while maintaining signal fidelity. The Texas Instruments ADS5474 shall be used as the ADC responsible for converting the feedback analog signal into the digital domain.

The ADS5474 is a high speed 14-Bit ADC that offers sample rates up to 400MSPS, offering a 305uV resolution and 16,384 states. Analogous to the DAC, the sample rate of the ADC was selected at 400MSPS to ensure sufficient margin to prevent signal aliasing of the 210MHz modulated signal.

With such a fine resolution, it is important to ensure the distortion characteristics of the ADC are as low as possible. The ADS5474 presents an INL of +/-1.0 bits and DNL of +/- 0.7 bits which defines the output amplitude error of up to +/- 305uV and state change errors of 305uV respectively.

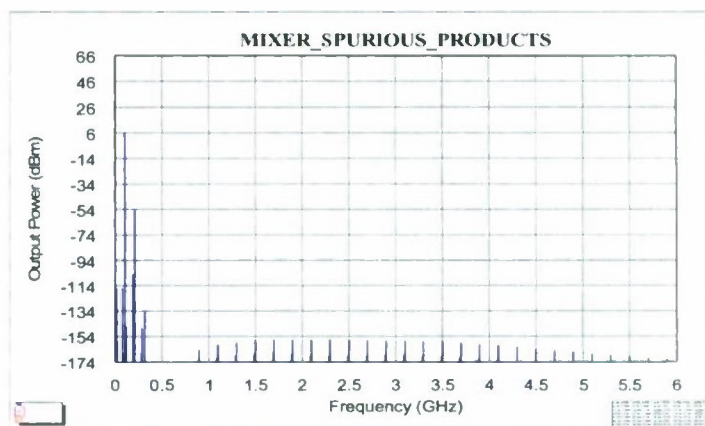


FIGURE 38: Out-of-Band Mixer Output Spurious Emissions

The fidelity of the digital signal is characterized by the ADCs SFDR, NSD, IMDs and ACPR. The ADS9474 is advertised [7] with a SFDR of -80dBc, harmonic distortion less than -60dBc, worst case NPD less than -157dBm/Hz and IMDs less than -70dBc. This describes the single and multi-carrier dynamic range of -70dBc by use of this ADC. With the incoming signal yielding spurious products at -60dBc, the use of the ADS9474 will not significantly contribute to the dynamic range limitations of the GC5325.

The net result is a feedback path that will offer very high linearity and introduce very low noise levels to the reference signal with a dynamic range limit of -60dBc. A reference signal can be down-converted with RF frequencies ranging between 30MHz through 4800MHz. Signal amplitude shall be controlled using a digitally controlled attenuator ensuring that all stages are properly driven and dynamic range is maintained with any modulation topology used. The high fidelity feedback signal will then be ready for re-sampling by the high speed ADC for proper DPD correction by the GC5325.

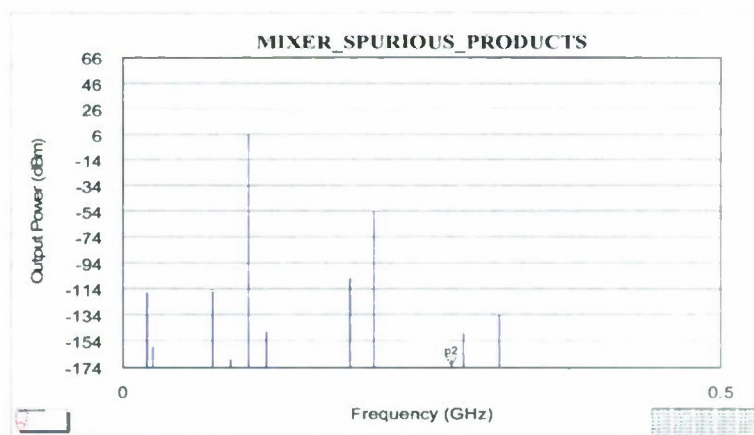


FIGURE 39: In-Band Mixer Output Spurious Emissions

SYSTEM OVERHEAD

Since the signal synthesis and correction aspects of the transmitter effectively result in static power overhead for the system, it is important to understand the total power consumption of the transmitter system. By implementing the signal conditioning and feedback system implementation discussed, the expected power overhead for the transmitter is 8.5W and can be summarized as shown in TABLE 3. Without efficiency enhancement techniques such as ET and using the data shown in FIGURE 22, FIGURE 23 and FIGURE 24, this would result in a typical transmitter efficiency of 48% while transmitting single carrier signals at 20W RF output power, 35% efficiency while transmitting multi-carrier signals with 3dB PAR at 10W RF output power and 20% efficiency while transmitting complex signals such as WCDMA with 13dB PAR with 6dB CFR. The efficiencies are expected to increase with the application of ET to 40% with multi-carrier modulation and 26% with WCDMA modulation.

MANUFACTURER	PART NUMBER	FUNCTION	Voltage	Power
		Description	V	W
Actel	A2F060M3F1FGG256Y1	Microprocessor	1.5	0.006
Analog Devices	AD9122	DAC	3.3	1.1
Analog Devices	ADL5561	Buffer Amplifier	3.3	0.1
Hittite	HMC460LC5	Buffer Amplifier	8.0	0.6
Texas Instruments	TMS320C6727	DSP	3.3	1.0
Texas Instruments	TRF372017	IQ Modulator	5.0	1.2
Texas Instruments	GC5325	CFR/DPD/ET	3.3	1.9
Texas Instruments	ADS5474	ADC	5.0	2.5
TOTAL			8.5 W	

TABLE 3: Transmitter Static Power Consumption

SECTION VII: Power Supply Modulator

The power supply modulator section of the Wideband High Efficiency Transmitter shall be responsible for enhancing transmitter efficiency and decreasing the thermal loading of the system by implementing envelope tracking (ET) functionality. The ET functionality accomplishes this by providing supply power to the high efficiency power amplifier only when needed to amplify the time varying amplitude characteristics of the modulated signal. As an example, the amplitude characteristics of a 4-tone modulated signal can be seen in FIGURE 40 along with its peak and average power levels.

Conventional power amplifiers are provided a fixed supply voltage which allows the device to amplify the time varying signal characteristics as needed. As a result, typical device efficiencies are 30% resulting in a significant portion of the supply power being dissipated as heat. By dynamically controlling the supply voltage to the high efficiency power amplifier, power is made available only when needed to sustain the RF envelope requirements. This allows the amplifier to operate at saturation for both low and high instantaneous output power states maximizing transistor efficiency with demonstrated values of 50% [8]. Concurrently, less power is lost as heat since the amplifier is not statically dissipating supply power. This dissipated power is detailed in FIGURE 40 as the region between the peak power level (Black Reference Line) and the signal envelope characteristics (Orange Reference Line).

To implement envelope tracking, the envelope amplitude characteristics of the modulated signal must be applied to the transistors supply power and aligned with the RF envelope signal. As an integrated feature of the GC5325, envelope amplitude characteristics are made available after DPD and CFR correction, based on the magnitude of the signals in-phase and quadrature components. These characteristics are provided to the microprocessor for use by the power supply modulator which is responsible for dynamically adjusting the supplied power to the transistor.

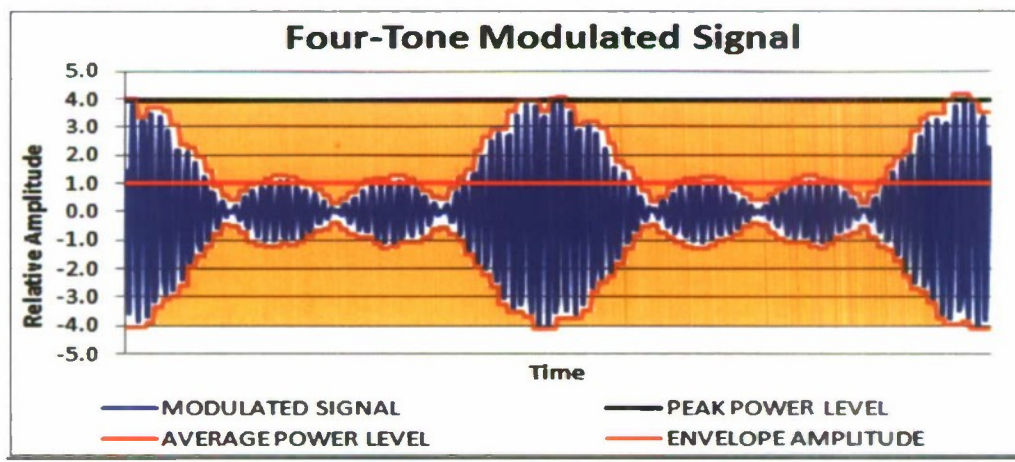


FIGURE 40: Time Domain Characteristics of a 4-Tone Modulated Signal

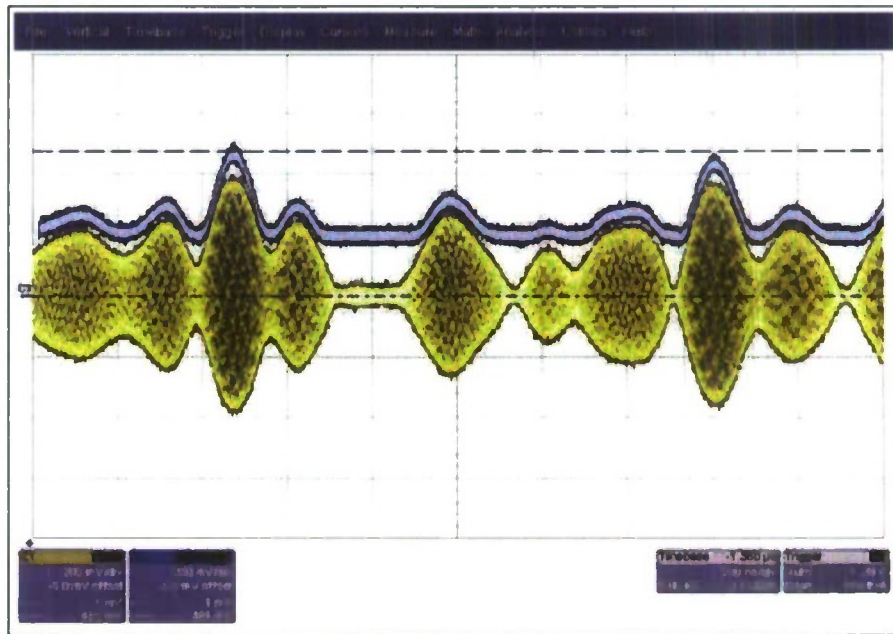


FIGURE 41: Power Supply Modulator Output and RF Envelope Signal Characteristics [8]

The power supply modulator shall be implemented as an integrated solution by utilizing the Nujira Ltd. Coolteq.h power supply modulator. This solution utilizes a proven, commercially available, highly linear, high voltage and high current sub-system supporting modulation bandwidths in excess of 20MHz. The power supply modulator shall be controlled by the microprocessor which provides the clock and modulated signal envelope characteristics from the GC5325. The microprocessor interfaces with the power supply modulator using a 14-pair parallel low voltage differential signal (LVDS) control line interface. The clock is provided by a single LVDS pair.

The power supply modulator shall control the supply voltage over a range of 10V to 28V allowing control for up to 10dB of RF amplitude variation. This effect is illustrated by Texas Instruments [8] and is illustrated in FIGURE 41 by evaluating the voltage variation (magenta curve) around the RF envelope (yellow curve). Since time alignment is critical in maximizing system efficiency, this function shall be software controlled by the microprocessor. By utilizing IP blocks from Texas Instruments, time alignment shall be automatically incorporated in the system ensuring optimum performance enhancements.

SECTION VIII: Demonstrated Prototype Results

The wideband high efficiency transmitter system utilizing the GC5325 digital pre-distortion, crest factor reduction and envelope tracking functionality can be leveraged from a system evaluation kit offered by Texas Instruments; the GC5325SEK. This system evaluation kit integrates the GC5325 processor and all necessary digital and analog circuitry to evaluate the performance of the transmit processor over frequencies extending between [700 – 2100]MHz. Though the bandwidth limits are smaller than the intended 30 - 6000MHz bandwidth objective of the wideband high efficiency transmitter, the demonstrated performance enhancements shall serve as a baseline to which the discussed transmitter implementation can expand the bandwidth limits to cover the full intended frequency range. As part of the system evaluation kit, multi-carrier WCDMA and LTE signals can be synthesized and evaluated with modulation bandwidths up to 20MHz. The development kit was provided as a courtesy by Texas Instruments to demonstrate feasibility of the proposed Wideband High Efficiency Transmitter.

Envelope Tracking features offer an integral part of the wideband transmitter system to enhance system efficiency. This functionality can be demonstrated by utilizing the Nujira High Accuracy Transmit (HAT) power supply modulator in conjunction with the GC5325SEK system evaluation kit. The GC5325SEK interfaces with the HAT modulator and provides the necessary instructions to control the power supply voltage available to the wideband power amplifier. The HAT modulator was provided as a courtesy by Nujira to demonstrate the feasibility of the proposed Wideband High Efficiency Transmitter.

As part of the development efforts, Aethercomm had procured and manufactured a limited functional high efficiency Class-J power amplifier consistent with the design implementation discussed. The power amplifier was manufactured using Monolithic Integrated Circuit (MIC) manufacturing processes to minimize extrinsic parasitic and size requirements. The prototype module was fabricated allowing functionality of Band 1 and Band 3 only in an effort to demonstrate the performance enhancements of the proposed power amplifier implementation. Band selection is achieved with the limited functional power amplifier by physically bridging the parallel tuning network to ground when enabling the corresponding band and as such does not include the diode switch elements.

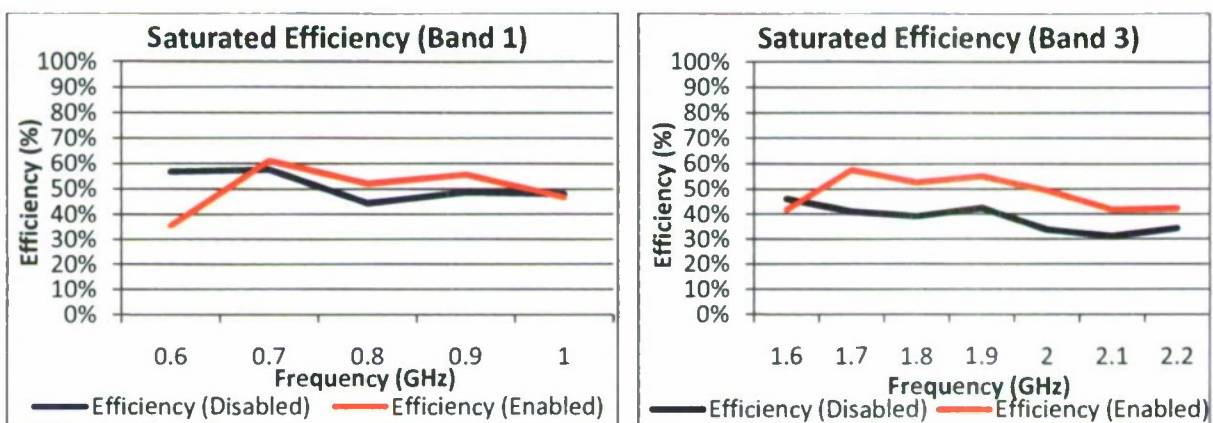


FIGURE 42: Measured Prototype High Efficiency Power Amplifier Efficiency Performance

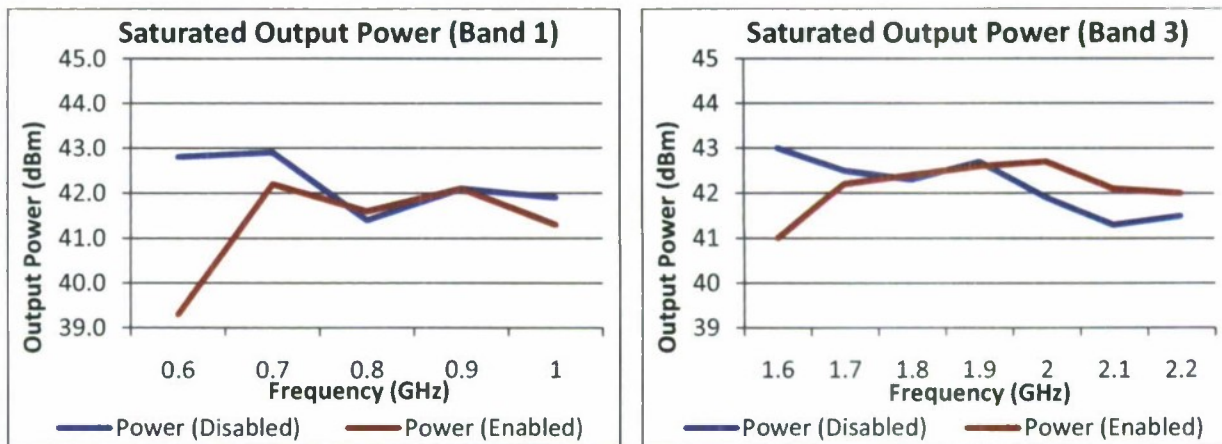


FIGURE 43: Measured Prototype High Efficiency Power Amplifier Output Power Performance

Since the efficiency improvements of the transmitter system are predicated on the high efficiency power amplifier, the CW performance was evaluated for each band. The results were evaluated with and without the corresponding band enabled to show the impact the tuning networks present to the RF transistor. Shown in FIGURE 42 and FIGURE 43 are the corresponding saturated performances for efficiency and output power, respectively. As can be seen, by implementing the switched high efficiency power amplifier tuning networks, the saturated efficiencies are typically 10% higher demonstrating that the high efficiency power amplifier design methodology is well suited to provide enhanced efficiency performances. Further efficiency refinement will be conducted during the next program development phase.

The high efficiency power amplifier was integrated with the GC5325SEK development platform to evaluate the non-linear behavior using complex modulation topologies. The corresponding non-linear behavior was then corrected using the integrated DPD functionality of the development kit. The GC5325SEK was configured so that the maximum PAR of the modulated signal shall not exceed 7dB. The various modulation signals were evaluated with an average output power of +34dBm and operated at 880MHz as defined in TABLE 4 with Band 1 enabled. Overall, the GC5325 transmit processor improves the high efficiency power amplifier non-linearity by at-least 13dBc yielding significant signal enhancement capabilities from the transmit processor.

The various modulation signals were evaluated with an average output power of +34dBm and operated at 2000MHz as defined in TABLE 5 with Band 3 enabled. Overall, the GC5325 transmit processor improves the high efficiency power amplifier non-linearity by at-least 11dBc.

SIGNAL	CARRIERS	BW	NO DPD	DPD	ACPR No DPD	ACPR With DPD
TYPE	QTY	MHz	FIGURE	FIGURE	dBc	dBc
WCDMA	Two	10	44	45	-33	-46
WCDMA	Four	20	46	47	-32	-45
LTE	One	20	48	49	-32	-46

TABLE 4: High Efficiency Power Amplifier Modulated Signal Performance Summary (Band 1)

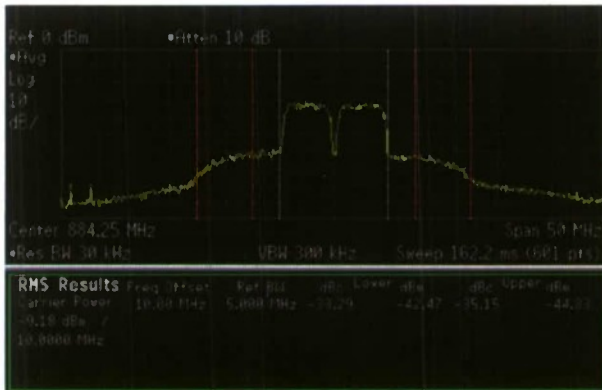


FIGURE 44: WCDMA without DPD

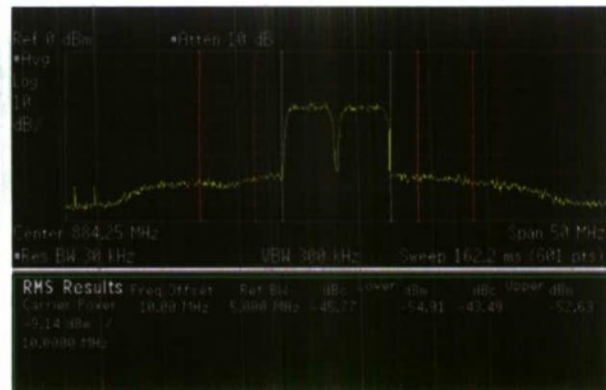


FIGURE 45: WCDMA with DPD

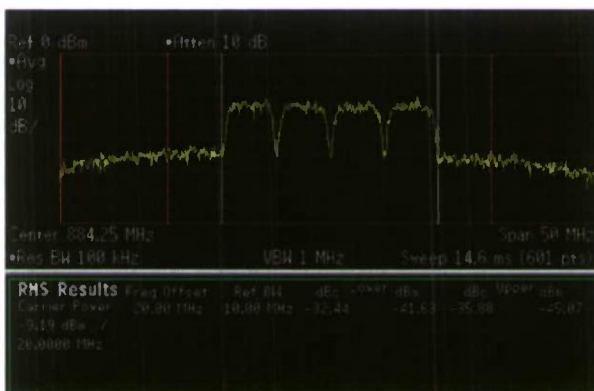


FIGURE 46: WCDMA without DPD

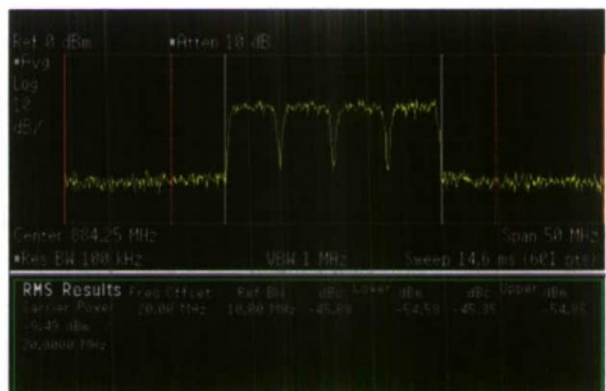


FIGURE 47: WCDMA with DPD

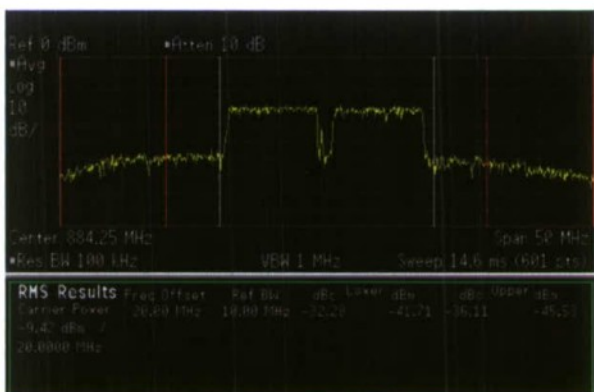


FIGURE 48: LTE without DPD

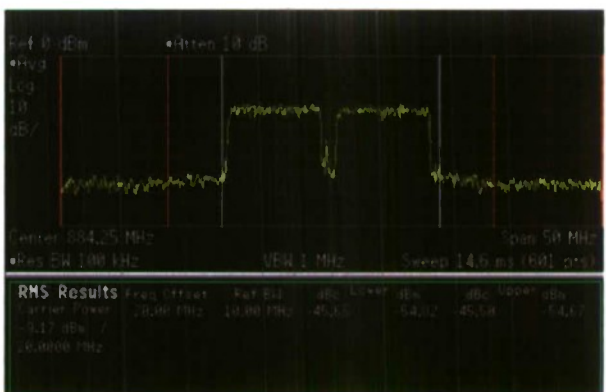


FIGURE 49: LTE with DPD

SIGNAL	CARRIERS	BW	NO DPD	DPD	ACPR No DPD	ACPR With DPD
TYPE	QTY	MHz	FIGURE	FIGURE	dBc	dBc
WCDMA	Two	10	50	51	-42	-55
WCDMA	Four	20	52	53	-40	-51
LTE	One	20	54	55	-40	-51

TABLE 5: High Efficiency Power Amplifier Modulated Signal Performance Summary (Band 3)

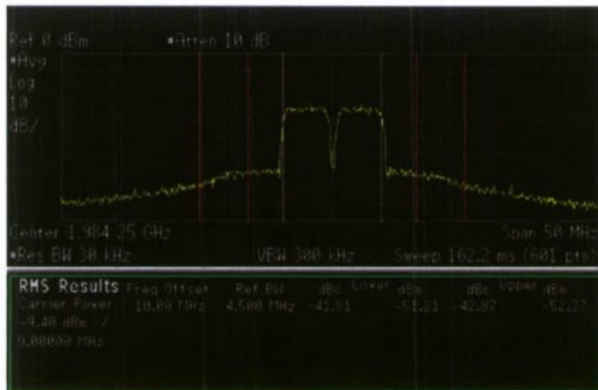


FIGURE 50: WCDMA without DPD

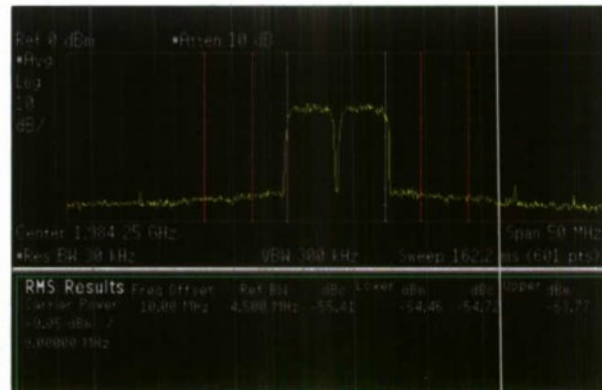


FIGURE 51: WCDMA with DPD

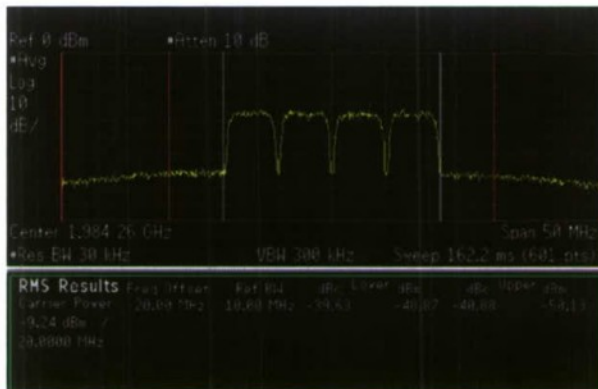


FIGURE 52: WCDMA without DPD

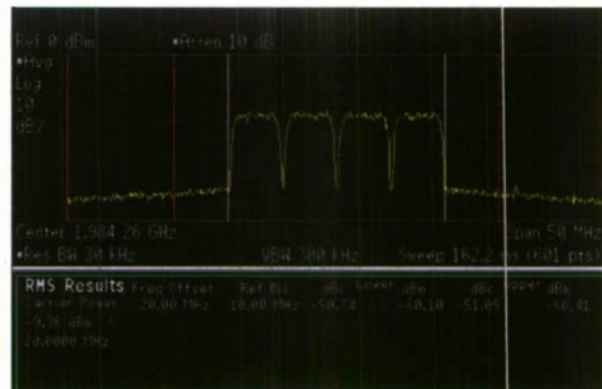


FIGURE 53: WCDMA with DPD

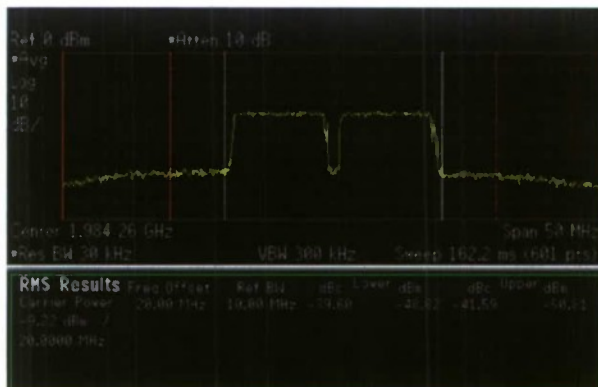


FIGURE 54: LTE without DPD

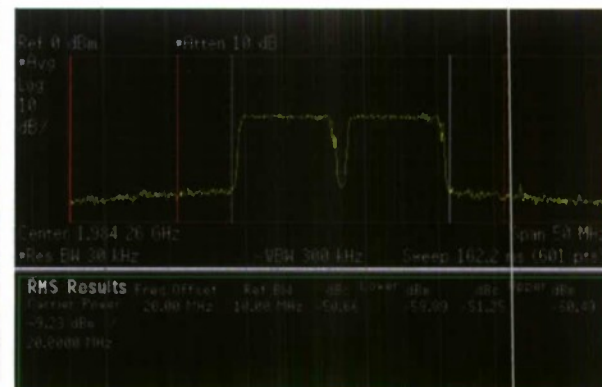


FIGURE 55: LTE with DPD

SECTION IX: Phase 2 Transition Plan

The Phase 1 development efforts have focused on the proof of concept for each of the sub-systems discussed in Section I. Detailed within this report are the available technologies and components that will achieve the Wideband High Efficiency Transmitter solution objectives in an integrated transmitter module. Simulated performances have been evaluated with emphasis on RF bandwidths covering two octaves around 1GHz while showing extended frequency capabilities to 30MHz.

Aethecomm has extensive history developing high efficiency power amplifier systems for many different communication platforms. This knowledge has been leveraged to produce a limited functional prototype of the high efficiency power amplifier during Phase 1 developments, which have been used to successfully demonstrate the power amplifier proof of concept. Therefore, the first development effort during the Phase 2 transition shall be to expand upon the proof of concept amplifier and build an integrated power amplifier module. The power amplifier module shall contain the necessary driver amplifiers and combine four high efficiency power amplifier final stages. The amplifier target shall be to achieve an average RF output power of +40dBm (10W) with emphasis on high peak-to-average complex modulations like WCDMA and standard modulation architectures used in typical HMS and GMR applications. The Phase 2 objective shall be to fully support frequencies ranging between 400MHz through 4000MHz and demonstrate extended operation down to 30MHz.

During Phase 1 developments, the proof of concept efforts has been further expanded by obtaining a system evaluation kit from Texas Instruments. The system evaluation kit is an integrated platform including a signal pattern generator, a DPD and CFR processor and all necessary components to synthesize complex signals at RF frequencies and demonstrate the spectral enhancement capabilities on them. The system evaluation kit has been applied to the limited functional high efficiency power amplifier and has successfully demonstrated signal fidelity enhancements while achieving improved efficiencies concurrently. The Phase 2 transition shall expand upon this system evaluation kit by integrating all digital signal conditioning, analog signal conditioning circuitry and linearity feedback circuitry detailed within this report into a single, modular assembly. This includes PWB layout considerations for high speed RF circuitry, integration of the high speed digital circuitry and applying necessary layout and filtering considerations. The design shall yield a high fidelity transmitter system with high spurious product rejection for both the main transmit path, ensuring a high fidelity signal is produced. The linearity feedback system shall provide a low noise signal with minimal introduced distortion to the digital signal conditioning circuitry for optimum, adaptive pre-distortion. The Phase 2 objective shall be to demonstrate spectral enhancement functionality from the module using various user-definable signals, comprised of simple or complex modulation architectures over the full operational frequency range of the high efficiency power amplifier.

The digital system integration shall address the user interface requirements that will provide seamless interface with existing GMR, HMS and other JTRS communication system platforms. During Phase 2 developments, the user interface will be established supporting digital baseband I/Q data containing encoded data with the desired modulation architecture. Timing considerations and various clock domains shall be identified and supported as necessary. The interface shall accept and interpret the user defined frequency, timing and sample rates between the user defined baseband data and the transmit processor. Use of standard blocks and proprietary (IP) blocks from Texas Instruments will be leveraged to maximize development efforts. This system integration shall also include definition and command structures for all frequency selectable system elements including the GC5325 IF frequency, IQ modulator synthesizer frequency and high efficiency power amplifier band selection networks.

The proof of concept efforts has further been expanded beyond the development of the high efficiency power amplifier and the Texas Instruments system evaluation kit by obtaining a High Accuracy Transmit (HAT) power supply modulator from Nujira Ltd. This modulator integrates directly to the Texas Instruments system evaluation kit and has successfully demonstrated Envelope Tracking efficiency enhancement capabilities on a Wideband high efficiency amplifier. These development efforts are to be leveraged during the Phase 2 development phase by incorporate the HAT power supply modulator into the transmitter assembly included with the high efficiency power amplifier, the digital and analog sections. The Phase 2 objective shall be to demonstrate Envelope Tracking efficiency enhancements as an integrated module including all components over the high efficiency power amplifier operating frequency ranges.

SECTION X: Conclusion

The cutting edge objective to create a Wideband High Efficiency Transmitter solution can be achieved with high signal fidelity and high efficiency. These features can be offered over bandwidths extending between 30MHz through 4000MHz. Using commercially available components available through Texas Instruments, Analog Devices, Nujira, Cree and Aeroflex, the technology is now available for Aethercomm to develop a high efficiency power amplifier and integrate it into a single transmitter solution for use in demanding mobile environments, with low thermal loading capacity and small form factors.

Aethercomm has shown that a high efficiency power amplifier can be developed to enhance efficiency over specific bands over frequencies ranging between 400MHz through 4000MHz with up to 67% efficiencies. These frequencies can be extended down to 30MHz and offer consistent performances by adding additional band functionality allowing support for both HMS, GMR and various commercial applications.

The high efficiency power amplifier performance levels shall be maintained with high PAR modulated signals such as multi-carrier, LTE, WiMAX and WCDMA by incorporating Envelope Tracking functionality in the transmitter. By using integrated features in the digital signal conditioning sub-system and utilizing the Nujira Coolteq.h power supply modulator, available power to the high efficiency power amplifier will be controlled so that supply power is available only when needed to sustain the modulated signal requirements and not lost as heat.

Enhanced signal fidelity will be provided by the Wideband High Efficiency Transmitter by implementing Digital Pre-Distortion. This functionality will be able to dynamically adapt and correct both simple and complex modulation topologies with PARs up to 13dB. Further efficiency improvements are realized by applying Crest Factor Reduction that reduce system overhead requirements and allow the high efficiency power amplifier to operate at higher output power levels.

Operation of the high efficiency power amplifier at higher average output powers are possible where the tradeoff is higher distortion and lower correction capabilities due to the strength of the non-linear products produced. By operating a single device at +34dBm, a total of four balanced transistors will be necessary to achieve the objective +40dBm (10W) average output power. Larger transistors can be used to reduce the combiner network complexity, but reduces the upper frequency capability of the wideband high efficiency transmitter.

With the design implementation proposed, the end product will be a rugged and robust, highly integrated, high efficiency, versatile, state-of-the-art transmitter solution suitable for fixed and mobile military platforms requiring high efficiency RF performance extending between 30MHz through 4000MHz.

SECTION XI: References

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